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 10oct02 10:44:34 User267149 Session D376.1

SYSTEM:OS  - DIALOG OneSearch
  File   2:INSPEC  1969-2002/Oct W1
         (c) 2002 Institution of Electrical Engineers
*File   2: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File   6:NTIS  1964-2002/Oct W1
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*File   6: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File   8:Ei Compendex(R)  1970-2002/Sep W5
         (c) 2002 Engineering Info. Inc.
*File   8: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File  34:SciSearch(R) Cited Ref Sci  1990-2002/Oct W2
         (c) 2002 Inst for Sci Info
*File  34: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File 434:SciSearch(R) Cited Ref Sci  1974-1989/Dec
         (c) 1998 Inst for Sci Info
  File  35:Dissertation Abs Online  1861-2002/Sep
         (c) 2002 ProQuest Info&Learning
  File  65:Inside Conferences  1993-2002/Oct W1
         (c) 2002 BLDSC all rts. reserv.
  File  94:JICST-EPlus  1985-2002/Aug W1
         (c)2002 Japan Science and Tech Corp(JST)
  File  99:Wilson Appl. Sci & Tech Abs  1983-2002/Sep
         (c) 2002 The HW Wilson Co.
  File 144:Pascal  1973-2002/Oct W1
         (c) 2002 INIST/CNRS
  File 305:Analytical Abstracts  1980-2002/Sep W5
         (c) 2002 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate
removal, customized scheduling.  See HELP ALERT.
  File 315:ChemEng & Biotec Abs  1970-2002/Aug
         (c) 2002 DECHEMA
  File 350:Derwent WPIX  1963-2002/UD,UM &UP=200264
         (c) 2002  Thomson Derwent
*File 350: Alerts can now have images sent via all delivery methods.
See HELP ALERT and HELP PRINT for more info.
  File 347:JAPIO  Oct 1976-2002/Jun(Updated 021004)
         (c) 2002 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run.  See HELP NEWS 347 for details.
  File 344:Chinese Patents Abs  Aug 1985-2002/Sep
         (c) 2002 European Patent Office
  File 371:French Patents  1961-2002/BOPI 200209
         (c) 2002 INPI.  All rts. reserv.
*File 371: This file is not currently updating. The last update is 200209.
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Set     Items   Description
S1     899932   (INTEGRAT??????(3N)(CIRCUIT?????? OR LOOP? ?)) OR IC
S2     180151   CLOS??????(3N)(CIRCUIT?????? OR LOOP? ? OR PATH? ? OR ROUT-
             E? ? OR ELECTRODE? ?)
S3      22133   MC=(U11-D01A OR U13-D02 OR U13-D02A)
S4      38249   IC=(H01L-023/12 OR H01L-027/085 OR H01L-027/088 OR H01L-02-
             7/092)
S5      73369   CC=(B2220 OR B2570)
S6    1130695   S1:S5
S7      17069   (MULTICHIP? ? OR MULTI()CHIP? ?)(3N)(MODULE? ? OR ARRANGE?-
             ?????)
S8      21508   (MULTICHIP? ? OR MULTI()CHIP? ?)
S9     205551   (ONE OR FIRST OR TWO OR SECOND)(3N)(CHIP? ? OR LEAD? ? OR -
             FRAME? ?)
S10    225953   S7:S9
S11    205551   (ONE OR FIRST OR TWO OR SECOND)(3N)(CHIP? ? OR LEAD? ? OR -
             FRAME? ?)
S12     21982   (BOND?????? OR JOIN??????)(3N)(PAD? ? OR PADDING OR CUSHIO-
             N?????)
S13    226192   S11:S12
S14    120373   (STACK?????? OR MOUNT??????)(3N)(CHIP? ? OR LEAD? ? OR FRA-
             ME? ?)
S15     47830   (BOND?????? OR JOIN??????)(3N)WIRE??????
S16      6705   (BONDWIR??????? OR WIREBOND???? OR (WIRING OR WIRE????)(N)-
             BOND???)(3N)(CHIP? ? OR LEAD? ? OR FRAME? ?)
S17     48014   S15:S16
S18    588123   (ONE OR FIRST OR TWO OR SECOND)(3N)(LAYER??? OR FILM??? OR
             COAT??? OR MULTILAYER??? OR SPACER???)
S19     98755   (ATTACH?????? OR CONNECT??????)(3N)(LAYER??? OR FILM??? OR
             COAT??? OR MULTILAYER??? OR SPACER???)
S20    664218   S18:S19
S21    108938   THERMOSET??????
S22       119   THERMOSET??????(3N)(PLIAB?????? OR BENT OR BEND??????)
S23    768148   S20:S21
S24     40973   (COUPL??????? OR LINK??????)(3N)(CHIP? ? OR LEAD? ? OR FRA-
             ME? ?)
S25      4355   ELECTRIC??????(3N)DISCONNECT??????
S26   1000880   DISCONNECT?????? OR GAP? ?
S27   1000880   S25:S26
S28     26090   S6 AND S10
S29     16401   S28 AND S13
S30      1694   S29 AND S14
S31       276   S30 AND S17
S32        45   S31 AND S20
S33        45   S32 AND S23
S34         2   S33 AND S24
S35        43   S33 NOT S34
S36         1   S35 AND S27
S37        42   S35 NOT S36
S38         9   S37 AND S8
S39         7   RD (unique items)
S40        33   S37 NOT S38
S41        10   S40 AND S12
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S42	10	S41 AND S15
S43	10	RD (unique items)
S44	23	S40 NOT S43
S45	18	S44 AND S18
S46	0	S45 AND S24
S47	0	S45 AND S25
S48	13	S45 AND S1
S49	13	RD (unique items)
S50	5	S45 NOT S49
S51	5	RD (unique items)
S52	5	S44 NOT S45
S53	5	RD (unique items)
S54	17466	S10 AND S14
S55	626	S54 AND S27
S56	41	S55 AND S20
S57	41	RD (unique items)
S58	41	IDPAT (sorted in duplicate/non-duplicate order)
S59	40	IDPAT (primary/non-duplicate records only)
S60	1	S59 AND S24
S61	39	S59 NOT S60
S62	1	S61 AND S16
S63	38	S61 NOT S62
S64	14	S63 AND S19
S65	7	S64 AND S18
S66	7	RD (unique items)
S67	7	S64 NOT S66
S68	7	RD (unique items)
S69	24	S63 NOT S64
S70	24	S69 AND S27
S71	0	S70 AND S25
S72	0	S70 AND S16
S73	1	S70 AND S15

34/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012056295
WPI Acc No: 1998-473206/199841
XRPX Acc No: N98-369508
Lead frame member for BGA resin sealed semiconductor device - includes conductive frame that supports heat resistant insulating material, is fixed to **one** peripheral surface of **lead** frame
Patent Assignee: DAINIPPON PRINTING CO LTD (NIPQ)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10200009	A	19980731	JP 9711850	A	19970108	199841	B

Priority Applications (No Type Date): JP 9711850 A 19970108
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10200009	A		10	H01L-023/12	

Abstract (Basic): JP 10200009 A

The lead frame member (100) includes a die pad (111) on which a semiconductor device is **mounted**. An inner **lead** (112) is electrically connected with terminal of the semiconductor device using **bonding wire**. An external terminal (113) integrally **coupled** with the inner **lead** is electrically connected with an external circuit. A lead frame (110) comprising die pad, inner lead, external terminal and a peripheral portion (114) is formed by plating. An aperture is provided, so that external terminal area is exposed.

One surface of the **lead** frame is covered and a heat resistant insulating material (120) is provided on its peripheral portion. A conductive frame (130) which supports the insulating material, is fixed to the near other peripheral surface of the lead frame.

USE - For ASIC in microcomputer, digital signal processor.

ADVANTAGE - Corresponds to multi-termination of **one layer** of semiconductor device and high density wiring.

Dwg.1/8

34/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008833079
WPI Acc No: 1991-337096/199146
XRPX Acc No: N92-284754
Encapsulated semiconductor device with partic. chip pad structure - has chip pad having conducting pattern, chip with electrode pads and leads connected via conducting pattern to pads
Patent Assignee: HITACHI LTD (HITA)
Inventor: KAWAI S; KITANO M; KOHNO R; NISHIMURA A; YAGUCHI A
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 3227541	A	19911008	JP 9023457	A	19900201	199146	B
US 5159434	A	19921027	US 91649712	A	19910201	199246	
US 5293068	A	19940308	US 91649712	A	19910201	199410	
			US 92959613	A	19921013		

Priority Applications (No Type Date): JP 9023457 A 19900201
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5159434	A		14	H01L-023/12	
US 5293068	A		14	H01L-039/02	Cont of application US 91649712 Cont of patent US 5159434

Abstract (Basic): US 5159434 A

The device comprises the semiconductor chip having electrode pads to be **coupled** to the **chip** pad and leads connected via the conducting pattern to the electrode pads. The chip pad, the chip and at least a portion of the leads are encapsulated. Through-holes are formed in the chip pad at positions corresp. to the electrode pads. The conducting pattern is formed on an insulating coat formed on the chip pad.

The semiconductor **chip** is **mounted** on a surface of the chip pad opposite to a surface on which the conducting pattern is formed in such a manner that the electrode pads face towards the through-holes. The electrode pads are electrically connected to the conducting pattern by first conducting members provided within the through-holes and the conducting pattern is electrically connected to the **leads** by **second** conducting members.

ADVANTAGE - Terminal arrangement of external leads is freely changeable at mfg. stage, esp. **wire bonding** stage, without modifying **chip**. Electrode pads need not be arranged in regular form with chip. Improved degree of freedom in design. High packaging density can be achieved. Compact. (First major country equivalent to JP3227541)

Dwg.2/18

JP 3227541 A

Newsprint, of several layers, is obtd. by forming outer layers maily of chemical pulp on both sides of an inner layer contg. de-inked pulp (DIP) and mechanical pulp in the wire parts of printing machines.

Alternatively, offset printing newsprint consisting of several layers is obtd. by forming an inner layer and outer layers contg. larger ratio of fines than the inner layer.

ADVANTAGE - The newsprint has high surface strength, brightness and stiffness.

In an example, paper of **one** inner **layer** and **two** outer **layers** was made with an oriented sheet former. The inner layer consisted of 18.75% GP, 37.5% TMP, and 43.75% DIP, and the outer layers consisted of 100% softwood BKP. The ratio of the inner layer to the outer layers was 80/20. The paper had (1) Clark stiffness of 40.4, (2) brightness of 52.7. (6pp Dwg.No.0/6)

Abstract (Equivalent): US 5293068 A

A chip pad has a conductive pattern, and a semiconductor **chip** has at least **one** electrode pad to be **coupled** to the **chip** pad. At least **one lead** is connected via the conductive pattern to the electrode pad. The chip pad, the chip and at least a portion of the leads are encapsulated. At least one through-hole is formed in the chip pad at a position corresponding to the electrode pad of the semiconductor chip. The conductive pattern is formed on an insulating coat formed on the chip pad.

The semiconductor **chip** is **mounted** on a surface of the chip pad opposite to a surface on which the conductive pattern is formed such that the electrode pad faces towards the through-holes. The electrode pad of the semiconductor chip is electrically connected to the conductive pattern by a first wire provided within the through-hole. The conductive pattern is electrically connected to the **leads** by at least **one** second wire.

USE/ADVANTAGE - Also applicable to TAB and CCB - Controlled Collapse Bonding. Terminal arrangement of external leads is freely changeable at **wire bonding** mfg. stage, without modifying chip. PCB may be designed compact. Electrode pads can be arranged at any position without consideration of subsequent mfg. processes.. Chip having LOC - lead on **chip** - structure can be **mounted** on **lead frame**.

Dwg.4/18

36/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012644140
WPI Acc No: 1999-450245/199938
XRPX Acc No: N99-336726
Semiconductor device with ball grid array BGA package - has solder resist that coats wiring on main surface of package substrate, and solder resist interposed between solder resist for wiring and die bond material
Patent Assignee: HITACHI LTD (HITA)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11186440	A	19990709	JP 97352995	A	19971222	199938	B

Priority Applications (No Type Date): JP 97352995 A 19971222
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11186440	A		8	H01L-023/12	

Abstract (Basic): JP 11186440 A
NOVELTY - The semiconductor device has a solder resist (10) that coats a wiring (5) formed on the main surface of a package substrate (1). Another solder resist (11) is interposed between the solder resist (10) and die bond material (7a). A semiconductor **chip** (2) is **mounted** on the main surface of the package substrate through the die bond material. DETAILED DESCRIPTION - Bump electrodes (9) are attached at the bottom of the package substrate, and electrically connected to the wiring through a hole (8) formed at the inside layer of the package substrate. **Bonding wires** (6) electrically connect the semiconductor chip and the wiring. Resin (3) seals the semiconductor chip.
USE - None given.
ADVANTAGE - Reduces stress caused by thermal expansion coefficient difference between the package substrate and semiconductor **chip** since the **two layers** of solder resist absorb the generated stress. Prevents **disconnection** of wiring formed on package substrate. Has no increase in number of parts and does not need complicated erector for BGA. DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of the semiconductor device with BGA package.
(1) Package substrate; (2) Semiconductor chip; (3) Resin; (5) Wiring; (6) **Bonding wires**; (7a) Die **bond** material; (8) Hole; (9) Bump electrodes; (10,11) Solder resist.
Dwg.2/7

39/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

4904108 INSPEC Abstract Number: B9504-2250-064
Title: Fabrication, assembly, and characterization of stacked **multichip modules** using hot pressed, co-fired aluminum nitride
Author(s): Minehan, W.T.; Weidner, W.K.; Jensen, R.J.; Spielberger, R.K.; Jacobsen, W.F.; Speerschneider, C.J.
Author Affiliation: Coors Electron. Package Co., Chattanooga, TN, USA
p.356-61
Publisher: ISHM-Microelectron. Soc, Reston, VA, USA
Publication Date: 1994 Country of Publication: USA x+630 pp.
ISBN: 0 930815 39 4
Conference Title: Proceedings of 3rd International Conference on Multichip Modules (SPIE Vol.2256)
Conference Sponsor: ISHM-Microelectron. Soc.; Int. Electron. Packaging Soc.; Electron. Ind. Assoc.; et al
Conference Date: 13-15 April 1994 Conference Location: Denver, CO, USA
Language: English
Abstract: A three-dimensional interconnect structure utilizing MCM-C technology is currently being developed by Honeywell Solid State Electronics Center (SSEC) and Coors Electronic Package Company. This concept involves the stacking of double sided co-fired aluminum nitride (AlN) MCMs. The double sided MCMs are stacked vertically using solder **attached** co-fired AlN **spacer** bars that have been manufactured with metallized through vias and have been designed to incorporate all electrical interconnection within the ceramic. The spacer bar acts as a thermal and electrical interconnect between substrates. Prototypes are currently being produced and evaluated for thermal, electrical, and mechanical integrity. Two technology characterization vehicles (TCVs) have been designed and constructed; the first TCV contains 6 metal layers and sites for **wirebond**, tape automated **bonding** (TAB), and flip **chip mounting**. A **second** characterization vehicle contains 15 metal planes and additional electrical characterization features. This paper will discuss the fabrication and assembly of the two TCVs. This Three-Dimensional Interconnect Structures Program is being funded by Naval Command, Control and Ocean Surveillance Center (NCCOSC).
Subfile: B

39/3,AB/3 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02220997 JICST ACCESSION NUMBER: 94A0724068 FILE SEGMENT: JICST-E
Special Articles: Recent Trends on MCM and Bare LSI **Chip** **Mounting**. Worldwide Trends of MCM/LSI Packaging Technologies.
HONDA TATSUO (1)
(1) Honda Jimusho
Sakitto Tekunoroji(Electronic Circuit & Packaging Technology), 1994, VOL.9,NO.5, PAGE.347-353, FIG.10
JOURNAL NUMBER: X0497AAN ISSN NO: 0914-8299
UNIVERSAL DECIMAL CLASSIFICATION: 621.315.5 621.382.049.77
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: A packaging process is divided into three layers, that is, the layer zero wherein diffusion and wiring are made on a LSI **chip**, the **layer one** where a package of a LSI chip is completed, and the **layer two** where packaging is done on a printed circuit board. The paper describes recent changes in these layers. Then, the paper discusses BIP, a technique for forming bump for joining bore chips, the three-dimensional packaging technology and HDI (High Density Interconnect) of GE as examples of new technologies to be named layer 1st or layer 5th.

39/3,AB/6 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009696893
WPI Acc No: 1993-390446/199349
XRPX Acc No: N95-162349
Encapsulated semiconductor **multichip module** for **integrated circuits** - has wiring layers with large current capacity provided on insulating substrate together with **IC** chips, while wiring layers having small current capacity are formed on flexible insulating film
Patent Assignee: TOSHIBA KK (TOKE)
Inventor: ENDO K
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 5291489	A	19931105	JP 9294267	A	19920414	199349	B
US 5422515	A	19950606	US 9334868	A	19930319	199528	
KR 9612650	B1	19960923	KR 936092	A	19930413	199926	

Priority Applications (No Type Date): JP 9294267 A 19920414
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 5291489	A		6	H01L-023/538	
US 5422515	A		9	H01L-023/48	
KR 9612650	B1			H01L-023/48	

Abstract (Basic): JP 5291489 A
Dwg.2/11
US 5422515 A
The module includes an insulating substrate (23) having power supply wiring layers (24). A number of electronic components, e.g. **IC chips**, are **mounted** on the substrate, via mount beds (25), and have **bonding pads**. An insulating sheet (28) provided above the substrate covers the electronic components and has small current wiring layers (29).
A number of apertures (30) are formed in the insulating sheet through which the power supply and small current wiring **layers** are electrically **connected** via **bonding wires** (33).The small current wires function as signal lines.
ADVANTAGE- Module has good heat dissipation and large current density. Efficiency of chip occupying area is increased as wiring area is reduced and number of chips is increased.
Dwg.6/10

43/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014507511
WPI Acc No: 2002-328214/200236
XRAM Acc No: C02-094771
XRPX Acc No: N02-257483
Continuous strip of sheet-like material for use in fabricating **integrated circuit** leadframes, includes base metal having adherent layer comprising nickel on both surfaces, and palladium adherent layers
Patent Assignee: TEXAS INSTR INC (TEXI); ABBOTT D C (ABBO-I); MITCHELL M E (MITC-I); MOEHLE P R (MOEH-I)
Inventor: ABBOTT D C; MITCHELL M E; MOEHLE P R
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020003292	A1	20020110	US 2000216548	P	20000707	200236 B
			US 2001900080	A	20010706	
JP 2002064173	A	20020228	JP 2001208345	A	20010709	200236

Priority Applications (No Type Date): US 2000216548 P 20000707; US 2001900080 A 20010706
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020003292	A1		11	H01L-023/495	Provisional application US 2000216548
JP 2002064173	A		10	H01L-023/50	

Abstract (Basic): US 20020003292 A1
Abstract (Basic):
NOVELTY - A continuous strip of sheet-like material, having two opposite surfaces, comprises a base metal having an adherent layer comprising nickel covering both the surfaces of the base metal. A palladium adherent layer is on the nickel **layer** of the **first** surface. A palladium adherent layer is on the nickel **layer** of the **second** surface.
DETAILED DESCRIPTION - A continuous strip of sheet-like material, having two opposite surfaces (11, 12), for use in fabricating **integrated circuit** leadframes, comprises a base metal (10) having an adherent layer comprising nickel covering both the surfaces of the base metal. A palladium (Pd) adherent **layer** having **first** thickness is on the nickel **layer** of the **first** surface. A Pd adherent **layer** having **second** thickness is on the nickel **layer** of the **second** surface. INDEPENDENT CLAIMS are also included for (A) a leadframe for use in the assembly of **integrated circuit** chips, comprising a structure stamped from the sheet so that the stamped edges extend between the surfaces, and the edges expose the base metal; (B) an **integrated circuit** (**IC**) device comprising the leadframe, an **IC chip mounted** to the **mount pad**, **bonding wires** interconnecting the **chip** and the **first** ends of

the **lead** segments, and encapsulation material surrounding the **chip**, **bonding wires** and the **first** ends of the **lead** segments, while leaving the second ends of the segments exposed, thus optimum adhesion to molding compounds is enabled; and (C) a method for fabricating a leadframe structure comprising selecting a continuous strip of sheet-like base material, plating of nickel on both surfaces, plating a Pd **layer** on the **first** surface in a thickness suitable for **bonding wire attachment**, plating a Pd **layer** on the **second** surface in a thickness suitable for parts attachment, and stamping the structure from the plated sheet.

USE - For use in fabricating **integrated circuit** leadframes.

ADVANTAGE - The strip provides low-cost, reliable mass production of leadframes.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic cross section of a portion of the continuous strip.

Base metal (10)

Opposite surfaces (11, 12)

pp; 11 DwgNo 1/4

43/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014446804
WPI Acc No: 2002-267507/200231
XRPX Acc No: N02-208001
Semiconductor device e.g. large scale **integrated circuit** has wiring **layer** sandwiched between **two** semiconductor **chips**, with **bonding pads** to connect **bonding wires**
Patent Assignee: NEC CORP (NIDE)
Inventor: FURUSAWA K
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020024146	A1	20020228	US 2001939761	A	20010828	200231	B
JP 2002076250	A	20020315	JP 2000259227	A	20000829	200234	

Priority Applications (No Type Date): JP 2000259227 A 20000829
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020024146	A1		8	H01L-023/48	
JP 2002076250	A		5	H01L-025/065	

Abstract (Basic): US 20020024146 A1
Abstract (Basic):
NOVELTY - A wiring layer (7) is sandwiched between **two** semiconductor **chips** (2,3) **stacked** on a substrate (1). The **bonding pads** (71a,71b) for connecting the **bonding wires** (14a,14b) are formed on the wiring layer.
USE - E.g. LSI circuit with memory and gate array.
ADVANTAGE - The wire length is shortened to prevent the wire sagging by its self weight and tilting of the wire at the time of sealing, so the deterioration of the wire strength is prevented.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the semiconductor device.
Substrate (1)
Semiconductor chips (2,3)
Wiring layer (7)
Bonding wires (14a,14b)
Bonding pads (71a,71b)
pp; 8 DwgNo 1/8

39/3,AB/7 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009693359
WPI Acc No: 1993-386913/199348
XRPX Acc No: N93-298781
Structure for packaging **IC** devices on **multi-chip modules** - has chip secured to substrate and electrically connected and subsequent **chips stacked** to desired height
Patent Assignee: NCHIP INC (NCHI-N)
Inventor: BRATHWAITE N E; FLATOW K; MARELLA P; TUCKERMAN D B
Number of Countries: 041 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9323982	A1	19931125	WO 93US4416	A	19930510	199348	B
AU 9342426	A	19931213	AU 9342426	A	19930510	199413	
US 5804004	A	19980908	US 92881452	A	19920511	199843	
			US 94300575	A	19940902		
			US 96655338	A	19960524		

Priority Applications (No Type Date): US 92881452 A 19920511; US 94300575 A 19940902; US 96655338 A 19960524
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9323982	A1	E	27	H05K-007/06	
Designated States (National): AT AU BB BG BR CA CH CZ DE DK ES FI GB HU JP KP KR LK LU MG MN MW NL NO NZ PL PT RO RU SD SE SK UA US					
Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL OA PT SE					
AU 9342426	A			H05K-007/06	Based on patent WO 9323982
US 5804004	A			H05K-003/32	Cont of application US 92881452 Div ex application US 94300575

Abstract (Basic): WO 9323982 A

The structure is for **stacking IC chips** (150a-150c). A **first chip** is secured to a silicon circuit board (160) with a layer of adhesive (170), and the others with an interstitial layer of thermally conductive and electrically non-conductive adhesive (188). Electrical connection is made via **wires** (189,190) to **bond pads** (180,192).

In fabrication, the **first chip** is secured to the circuit board, and **wire-bonded** to the **bond pads** (18), which provide contacts through vias for **connection** to interconnect **layers** (182) and conducting plane (183) containing power, and ground planes (184,186) of the silicon circuit board. Each **chip** is **stacked** and similarly connected to respective **bond pads**, which may be staggered to facilitate wire removal if necessary.

ADVANTAGE - Provides structure for reducing size and complexity of **multi-chip modules** with less cost and technological risk.

39/3,AB/5 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010202167
WPI Acc No: 1995-103421/199514
XRAM Acc No: C95-047668
XRPX Acc No: N95-081532
Semiconductor device for information processing apparatus - has multilayer wiring board which uses polyimide **film layers** **connected** to **bond pads** firmly through holes separated by inorganic material
Patent Assignee: FUJITSU LTD (FUIT)
Inventor: MOTOYAMA T
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7030012	A	19950131	JP 93169461	A	19930709	199514	B
US 5621246	A	19970415	US 94217110	A	19940324	199721	

Priority Applications (No Type Date): JP 93169461 A 19930709
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7030012	A		6	H01L-023/12	
US 5621246	A		14	H01L-023/48	

Abstract (Basic): JP 7030012 A

The semiconductor device has a **first** quality **layer** of inorganic material on the surface used as substrate. An insulation layer which consists of an organic matter is formed over the semiconductor substrate. On top of it, a **multilayer** inter **connection layer** consisting of conductive material is formed. A **bonding pad** provided in the **multilayer** interconnection **layer** is **connected** to the external surface electrically through an opening (12) provided at the insulation layer.

The **bonding pad** consists of second quality conductive inorganic material. The semiconductor substrate and pad metal layer are stuck firmly by the quality of inorganic materials content moisture is omitted from the opening (13) at the time of curing. The peripheral part of a pad domain is formed in the shape of stairs by the polyimide layer.

ADVANTAGE - Improves speed of information processing apparatus. Reduces size. Improves sticking intensity in pad domain. Eliminates cracks in film forming and heterogeneity of films.

Dwg.3/6

Abstract (Equivalent): US 5621246 A

A **multichip** substrate for **mounting IC** semiconductor **chips**, comprises: a base substrate a **first** insulation **layer** fabricated on the base substrate; multi-insulation **layers** accumulated on the **first** insulation **layer**; multi-wiring layers made of an electrically conductive substance, accumulated on the **first** insulation **layer**, interposing the multi-insulation layers into the multi-wiring layers

for keeping the multi-wiring layers apart; a **bonding pad** for external electrical connection of **multi chip** substrate made of an electrically conductive substance, lying above the multi-insulation layers and the multi-wiring **layers** and electrically **connected** with the multi-wiring layers through the multi-insulation layers; and standing structures made by accumulating **first** substance **layers** so as to stand between the **bonding pad** and the **first** insulation **layer** in at least a bonding region of the **bonding pad** and under the **bonding pad**, passing through the multi-insulation layers, so as to stick to the **first** insulation **layer**, the bonding region being a region in which **wire bonding** is carried out.

Dwg.1/7

39/3,AB/4 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010233560
WPI Acc No: 1995-134817/199518
XRPX Acc No: N96-081694

Multi-chip module - has thin film multilayer interconnection part over ceramic substrate having thick film wiring layer between them and semiconductor chips connected by **bonding pads**

Patent Assignee: TOSHIBA KK (TOKE)
Inventor: ITO K
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7058240	A	19950303	JP 93203808	A	19930818	199518	B
US 5488542	A	19960130	US 94291859	A	19940817	199611	

Priority Applications (No Type Date): JP 93203808 A 19930818
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7058240	A		6	H01L-023/12	
US 5488542	A		10	H05K-001/11	

Abstract (Basic): JP 7058240 A

The semiconductor device consists of a multilayer ceramic base substrate (10). Thin film multilayer interconnection part is formed by forming thin film wiring layer (30) over thin film insulation layer alternatively. A semiconductor chip (40) placed over the thin **film** wiring part is **connected** by **bonding wire** (41) between **chip side bonding pad** (42) and substrate side **bonding pad** (33). A thick **film** wiring **layer** (20) formed between the multilayer ceramic substrate and **the** thin **film** wiring **layer** is **connected** to the thin **film** wiring layer by thick film wiring pad (25).

ADVANTAGE - Prevents short circuiting of **bonding pad. Improves** wiring density. Improves **characteristic** of device. Reduces cost.

Dwg.1/10

US 5488542 A

The module comprises a thick film wiring part (20) formed on the ceramic base substrate (10) with a thick film wiring layer and a thick film insulating layer. The thin film multilayered wiring part (30) formed on the thick film wiring part includes a first region in which thin film wiring layers and thin film insulating layers are alternately stacked upon each other. A second region includes a number of thin film insulating **layers** are stacked upon **one** another.

One of the thin **film** wiring **layers** of the **first** region thin **film multilayer** wiring part is electrically connected to **one** of the thin **film** wiring layers of the thin film multilayered wiring part using part of the thick film wiring **layers** located under the **second** region. A semiconductor **chip** is **mounted** on the thin film multilayered

wiring part which includes a number of **bonding pads**. A connection wiring electrically connects the **bonding pads**.

USE/ADVANTAGE - Controls characteristic impedance by varying thickness of insulating layer. Prevents breakage of insulator due to bonding damage and short circuits between conductors. Increases density of wiring.

Dwg.2/10

39/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

4503567 INSPEC Abstract Number: B9311-0170J-015
Title: A laser-programmable **multichip module** on silicon
Author(s): Berger, R.; Frankel, R.S.; Raffel, J.I.; Woodward, C.E.; Wyatt, P.W.
Author Affiliation: MIT Lincoln Lab., Lexington, MA, USA
Conference Title: 1993 Proceedings. Fifth Annual IEEE International Conference on Wafer Scale Integration (Cat. No.93CH3227-6) p.30-5
Publisher: IEEE, New York, NY, USA
Publication Date: 1993 Country of Publication: USA ix+374 pp.
ISBN: 0 7803 0867 0
U.S. Copyright Clearance Center Code: 0 7803 0867 0/93/$3.00
Conference Sponsor: IEEE
Conference Date: 20-22 Jan. 1993 Conference Location: San Francisco, CA, USA
Language: English
Abstract: A laser-programmable substrate for **multichip modules** comprises a silicon substrate with a dense, predefined array of pads, tracks and links. A pattern of wiring connecting some of the pads is formed with a laser. **Integrated circuit chips** are **mounted** on the substrate, and the **chip pads** are **wire-bonded** to the substrate **pads**. East-west tracks are on the second level of metal, and north-south tracks on the first level. Power, ground, and signals share the tracks on the **two** metal **layers** . There is an array of 258-by-258 pads on a 200- mu m pitch, and there are three signal tracks, one power track, and one ground track between any two adjacent pads. Links consist of a silicon nitride **layer** sandwiched between the **two** metal **layers**. When a laser pulse of the correct power and duration is directed to the link region, the metal and nitride fuse to form a conductive vertical path, with a resistance typically two ohms.
Subfile: B

43/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014061965
WPI Acc No: 2001-546178/200161
XRPX Acc No: N01-406216
Semiconductor device in ball grid array package, has sealing materials which respectively seals **two** semiconductor **chips** **mounted** on both sides of wiring board
Patent Assignee: HITACHI LTD (HITA); HITACHI YONEZAWA DENSHI KK (HITA-N)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001210745	A	20010803	JP 200016586	A	20000126	200161	B

Priority Applications (No Type Date): JP 200016586 A 20000126
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001210745	A		10	H01L-023/12	

Abstract (Basic): JP 2001210745 A
Abstract (Basic):
NOVELTY - Wiring board (1) has wiring **layers** (10,11) electrically **connected** through a through-hole (9). Semiconductor chips (2,3) are respectively mounted to openings (12) in both surfaces of the board. **Wires** (4,5) are **bonded** between each **pad** on chips (2,3) respectively and wiring layers. Sealing materials (6,7) respectively seal the chips (2,3). An external terminal (8) is connected to the back side of the wiring layer (11).
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for semiconductor device manufacturing method.
USE - In ball grid array (BGA) package for large scale integrated (LSI) system.
ADVANTAGE - As the semiconductor **chips** are **mounted** through the openings in the wiring layer, the need for bonding the chips to the board is eliminated. Thus generation of curvature and distortion of board is prevented. As the semiconductor chip is formed on both sides of the wiring board, the size of the device is reduced due to the thin shape and hence attains cost reduction.
DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of the semiconductor device. (Drawing includes non-English language text).

Wiring board (1)
Semiconductor chips (2,3)
Wires (4,5)
Sealing materials (6,7)
External terminal (8)
Through-hole (9)
Wiring layers (10,11)
Opening (12)
pp; 10 DwgNo 3/8

43/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011782410
WPI Acc No: 1998-199320/199818
XRPX Acc No: N98-158371
Wiring structure of substrate for **mounting** bare **chip** - has ground wiring layer and power supply wiring **layer** which are **connected** to ends of ground tape and power supply tape respectively
Patent Assignee: OKI ELECTRIC IND CO LTD (OKID)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10050747	A	19980220	JP 96198621	A	19960729	199818	B

Priority Applications (No Type Date): JP 96198621 A 19960729
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10050747	A		5	H01L-021/60	

Abstract (Basic): JP 10050747 A

The structure has a **wire bonding pad** (22) arranged on the surface of a substrate (20) at the periphery of a bare chip (21). A ground tape (24) is arranged covering a part of the **wire bonding pad**. The ends of the tape are connected to the substrate. A power supply tape (27) arranged adjacent to the ground tape has both ends connected to the surface of the substrate. The ends of the ground tape are connected to a ground wiring **layer** (25g) through a **first** connection part (26g).

The ends of the power supply tape are connected to a power supply wiring **layer** (25v) through a **second** connection part (26v). The ground tape is **bonded** to a first **pad** which is formed on the bare **chip** corresponding to the **first** wiring **layer** . The power supply tape is **bonded** to a second **pad**, which is formed on the bare **chip** corresponding to the **second** wiring **layer**.

ADVANTAGE - Improves mounting efficiency. Prevents interference between connection parts.

Dwg.1/2

43/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011240961
WPI Acc No: 1997-218864/199720
XRPX Acc No: N97-180841
Ball grid array type semiconductor device e.g. **IC**, LSI - has lead frame conductor circuit pattern formed between **first** and **second** insulated **layers** through etching or press stamping processes
Patent Assignee: MITSUI HIGH TEC KK (MIHI)
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 9064225	A	19970307	JP 95240909	A	19950825	199720	B
JP 3115807	B2	20001211	JP 95240909	A	19950825	200101	

Priority Applications (No Type Date): JP 95240909 A 19950825
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 9064225	A		6	H01L-023/12	
JP 3115807	B2		5	H01L-023/12	Previous Publ. patent JP 9064225

Abstract (Basic): JP 9064225 A

The device (10) has a semiconductor **chip** (16) **mounted** on the surface of a semiconductor **chip mounting** substrate (14) which includes a conductor circuit pattern (13). Several conductor leads (11) and electrode pads (17) formed on the semiconductor chip surface, are connected through **bonding wire** (18). A dense sealing resin element (19) is provided on the side of the semiconductor **chip mounting** surface. A **first** insulated **layer** (23) provides a **first** opening (22) which exposes a **wire bonding pad** (21) and a semiconductor **chip mounting** stage (12).

A **second** insulated **layer** (26) provides a conducting hole (25) which exposes an external connection terminal island (24). The conductor circuit pattern of a lead frame is formed between the **first** and **second** insulated **layers** through press stamping or etching processes.

ADVANTAGE - Reduced manufacturing cost by maintaining shape and size of conductor lead pattern during early stages of manufacturing process. Protects conductor circuit pattern from deformation or chemical damage by coating conductor circuit pattern with resistant mask layer.

Dwg.1/3

43/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009166509
WPI Acc No: 1992-293943/199236
Related WPI Acc No: 1997-375146
XRPX Acc No: N92-225186
Miniaturised electronic circuit package for space exploration - has semiconductor chips connected to bus lines provided on substrate with die bonding ground **connected** through insulating **layer** by via holes
Patent Assignee: HITACHI LTD (HITA); HITACHI CHEM CO LTD (HITB); AKIYAMA M (AKIY-I); IHARA H (IHAR-I); KANEKAWA N (KANE-I); KAWABATA K (KAWA-I); OKISHIMA T (OKIS-I); YAMANAKA H (YAMA-I)
Inventor: AKIYAMA M; IHARA H; KANEKAWA N; KAWABATA K; OKISHIMA T; YAMANAKA H
Number of Countries: 008 Number of Patents: 015
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 501474	A2	19920902	EP 92103361	A	19920227	199236	B
JP 4273470	A	19920929	JP 9134038	A	19910228	199245	
CA 2061949	A	19920829	CA 2061949	A	19920227	199246	
EP 501474	A3	19930113	EP 92103361	A	19920227	199346	
US 5468992	A	19951121	US 92843234	A	19920228	199601	
US 5614761	A	19970325	US 92843234	A	19920228	199718	
			US 95523346	A	19950905		
CA 2061949	C	19980127	CA 2061949	A	19920227	199816	
US 5789805	A	19980804	US 92843234	A	19920228	199838	
			US 95523346	A	19950905		
			US 96746942	A	19961118		

Priority Applications (No Type Date): JP 9134038 A 19910228; JP 9846813 A 19910228; JP 99329217 A 19910228
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 501474	A2	E	15	H01L-023/538	
Designated States (Regional): DE FR GB IT NL					
JP 4273470	A		11	H01L-025/04	
CA 2061949	A			H01L-023/522	
EP 501474	A3			H01L-023/538	
US 5468992	A		13	H01L-023/28	
US 5614761	A		14	H01L-023/28	Cont of application US 92843234 Cont of patent US 5468992

Abstract (Basic): EP 501474 A
The electronic circuit comprises at least **two** semiconductor **chips** (101-106) which are connected to a bus line (100) and to one wiring substrate (10). The bus line includes two data bus lines, one for each side of the substrate.
The wiring substrate (10) may be a multilayer wiring substrate comprising an insulating layer partially formed on the surface of the substrate and a die bonding ground formed on the surface of the

insulating layer. Wiring conductors from a wiring pad and via holes are formed in the periphery and inside of the die bonding ground with wiring conductors connected to other wiring conductors through the holes.

ADVANTAGE - Provides small, light, apparatus which has high reliability.

Dwg.1/11

Abstract (Equivalent): US 5614761 A

An electronic circuit package, comprising:

a multilayer wiring substrate;

a plurality of semiconductor bare chips which are bare-**chip mounted** on said wiring substrate, wherein said semiconductor **chips** include a **first** memory;

a bus line which is formed on said wiring substrate; and

wire bonding pads formed on the semiconductor bare chip and wiring substrate;

wherein each of said plurality of semiconductor bare chips is electrically connected to said bus line through **wire bonding** connections between said **wire bonding pads** formed on the semiconductor bare chips and the wiring substrate,

wherein said bus line includes a first data bus line and a second data bus line, said first bus line being formed on one side of said wiring substrate, and said second data bus line being formed on the other side of said wiring substrate, and

wherein chips of said semiconductor bare chips, which are connected to said first data bus line, are formed on said one side of said wiring substrate and others of said semiconductor bare chips, which are connected to said second data bus line, are formed on said other side of said wiring substrate.

Dwg.2/10

US 5468992 A

An electronic circuit package comprising: a multilayer wiring substrate, wherein said multilayer wiring substrate includes internal wiring conductors; an insulating layer formed on a portion of a surface of said multilayer wiring substrate;

a plurality of die bonding grounds formed on a surface of said insulating layer; a plurality of semiconductor bare chips formed on said die **bonding** ground; wiring **pads** formed on said semiconductor bare chips and on said multilayer wiring substrate along the periphery of said die bonding ground, wherein said semiconductor bare chips are connected to said wiring conductors through **wire bonding** between **wire bonding pads** formed on said semiconductor bare chips and the wiring substrate; wherein a portion of said multilayer wiring substrate under said die bonding ground is used as a via hole region for affecting connection between said wiring conductors.

Dwg.2/10

43/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008652208
WPI Acc No: 1991-156237/199121
XRPX Acc No: N91-119959
Packaged electronic device e.g. **integrated circuit** - uses tape frame that is intermediate in inter connection structure between **wire bonds** from electronic component and lead frame
Patent Assignee: MOTOROLA INC (MOTI)
Inventor: CASTO J J
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5014113	A	19910507	US 89457444	A	19891227	199121	B
JP 4211152	A	19920803	JP 90417943	A	19901220	199237	

Priority Applications (No Type Date): US 89457444 A 19891227
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 4211152	A		6	H01L-023/50	

Abstract (Basic): US 5014113 A
The lead frame having multiple **layers** permits fine **connection** to a large number of **bonding pads** on an electronic component such as an **integrated circuit IC**), but strong external package leads. A fully featured or completely extensive lead frame layer bears proximal ends that may be finely dimensioned for connection with the **bonding pads** of an **IC**. A **second frame layer** is laminated with the **first layer**, but does not have proximal ends that extend as far as those of the fully featured frame layer.

The doubled external **leads** for **mounting** to a printed circuit board PCB) are relatively stronger than the single, more finely featured proximal lead ends that are bonded to the component. The lead frame layers may also differ with respect to their thicknesses, electrical conductivity, strength and solder-wetting characteristics.

ADVANTAGE - Has large number of interconnections i.e. high I/O count, while having finely dimensioned connections to **IC**, but more robus exterior package leads. (7pp Dwg.No.1/3)

43/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003699176
WPI Acc No: 1983-59159K/198325
XRAM Acc No: C83-057390
XRPX Acc No: N83-106604
Substrate for **mounting integrated circuit chips** - has some solder **pads** for direct **bonding** and some with multilayer pedestal for **wire bonding**
Patent Assignee: IBM CORP (IBMC)
Inventor: MARKS R; PHELPS D W; WARD W C
Number of Countries: 005 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 81135	A	19830615	EP 82110816	A	19821123	198325	B
JP 58101493	A	19830616				198330	
US 4447857	A	19840508	US 81328889	A	19811209	198421	
EP 81135	B	19870318				198711	
DE 3275789	G	19870423				198717	

Priority Applications (No Type Date): US 81328889 A 19811209
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 81135	A	E	12		
Designated States (Regional): DE FR GB					
EP 81135	B	E			
Designated States (Regional): DE FR GB					

Abstract (Basic): EP 81135 A

Substrate for **mounting IC chips**, having input and output pins (40) and a number of solder pads, (26,28) has (some of) the pads (26) arranged in a pattern for interconnecting an **IC** chip and includes at least one solder pad (28) **connected** to a **multilayer** metallic pedestal (30). The pedestal comprises (a) a solder layer (32) **joined** to the solder **pad**; (b) an upper layer (34) of metal suitable for bonding to Al or Au wire, pref. Al or Au; and (c) a layer (36) of metal between and impervious to the solder layer and upper layer, pref. Ni.

At least one gp. of solder pads are pref. arranged in a pattern to match and interconnect with the solder pads on at least **one** flip **chip IC** and either (i) at least **one** pad contacts the **multilayer pad** for **wire bonding**; or (ii) at least one second gp. of pads is provided arranged to interconnect with a selected configuration of a **wire bond** type **IC chip**, each pad of the second gp. being **connected** to a **multilayer** pedestal.

Arrangement allows both more than **one** type of **chip** to be packaged on a single substrate, and/or more than one type of connection to be made to a single chip.

2/4

43/3,AB/9 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06482833
SEMICONDUCTOR PLASTIC PACKAGE

PUB. NO.: 2000-068411 [JP 2000068411 A]
PUBLISHED: March 03, 2000 (20000303)
INVENTOR(s): TAKE MORIO
IKEGUCHI NOBUYUKI
KOBAYASHI TOSHIHIKO
APPLICANT(s): MITSUBISHI GAS CHEM CO INC
APPL. NO.: 10-250445 [JP 98250445]
FILED: August 20, 1998 (19980820)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a semiconductor plastic package with superior **connection** between an inner-**layer** metal core and an outer layer metal foil, heat radiation, heat resistance, after moisture absorption, etc.

SOLUTION: In a semiconductor plastic package with a ball grid array using both-sided truncated conical metal cores with both surfaces, truncated conical protrusions on the front surface and the rear surface are individually exposed between semiconductor **chip mounted** metal foils a and between metal foils for ball pads, respectively. After a desmearing treatment of the exposed metal surfaces, the entire surfaces are metal-plated and coated with a plating resist, excluding a semiconductor **chip mounting** part g, the **bonding pad** parts and ball pad parts. In the printed wiring board obtained by plating with a noble metal h, a metal core c and a through-hole f are insulated by a **thermosetting** resin composition such as multifunctional cyanate ester, etc. A semiconductor **chip** is fastened on **one** surface of the wiring board with a heat-conductive adhesive and the chip, **wires** and **bonding pads** are resin-sealed in this semiconductor plastic package.

43/3,AB/10 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

02644836
PRINTED WIRING BOARD

PUB. NO.: 63-261736 [JP 63261736 A]
PUBLISHED: October 28, 1988 (19881028)
INVENTOR(s): TSUNASHIMA EIICHI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-096549 [JP 8796549]
FILED: April 20, 1987 (19870420)
JOURNAL: Section: E, Section No. 719, Vol. 13, No. 81, Pg. 64, February 23, 1989 (19890223)

ABSTRACT

PURPOSE: To achieve high power consumption allowance, to make it possible to **mount two** electronic circuit **chips** used for dual circuits in holes in both surfaces of the same wiring board and to implement a compact configuration, by using a metal plate or a metal film as an inner conductor **layer, attaching multilayer** interconnection boards having the holes to both surfaces of the inner conductor layer, and **mounting** the electronic circuit **chips** in said holes.

CONSTITUTION: Aluminum is used for a metal plate, i.e., an inner conductor layer 10. As wiring boards, insulating layers 6 and 7 made of aramid-fiber epoxy-resin impregnated cloth and electrodeposited copper foils 9 and 11 are provided. Die bonding of semiconductor **integrated circuit** chips 1 and 3 on both surfaces is performed by silver paint 12 and its **thermosetting** . Wires 2 and 4 are gold wire. Holes 13 and 14 are provided. The thicknesses of the insulating layers 5, 6, 7 and 8 are changed by the thicknesses and the sizes of the semiconductor **integrated circuit** chips 1 and 3. The exposed parts of the conductor layers 9 and 11 are plated with silver and used as outer **pads** for the **bonding** of the **wires** 2 and 4. The hole parts can be filled with epoxy resin and the like.

49/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014403533
WPI Acc No: 2002-224236/200228
Related WPI Acc No: 2002-215562
XRAM Acc No: C02-068405
XRPX Acc No: N02-171701

Wire bond integrated circuit chip mounting method for semiconductor package, involves forming openings by coating build-up multi-**layer** as mask and **connecting** solder balls via openings

Patent Assignee: THIN FILM MODULE INC (THIN-N)
Inventor: HO C W
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6277672	B1	20010821	US 99389634	A	19990903	200228	B

Priority Applications (No Type Date): US 99389634 A 19990903
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6277672	B1		11	H01L-021/44	

Abstract (Basic): US 6277672 B1
Abstract (Basic):

NOVELTY - Interconnect layer and build-up multi-layer (BUM) are formed on dielectric layer of metal substrate as interconnect substrate (12) openings and cavities are formed on dielectric layer and other surface of metal substrate (14). Chips are inserted cavities in and **wire bonded** to openings BUM layer is coated as mask and openings are formed. Solder balls are inserted and connected via openings.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for interconnect substrate formation method.

USE - Mounting **wire bond integrated circuit chip** on substrate For ball grid array type semiconductor package

ADVANTAGE - By using build-up multi-layer technology in combination with thin film deposition techniques, high density package is obtained. Irrespective of warpage and dimensional variations during high temperature or wet chemical processing.

DESCRIPTION OF DRAWING(S) - The figure shows a single **wire-bond chip** package with **two** interconnect **layers**.

Interconnect substrate (12)
Metal substrate (14)
pp; 11 DwgNo 1/3

49/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014056782
WPI Acc No: 2001-540995/200160
Related WPI Acc No: 2002-040077
XRAM Acc No: C01-161404
XRPX Acc No: N01-402090
Mounting of flip **chip** on metal substrate, involves forming opening on exposed build-up multi-**layer** on **one** side, and openings on other side of substrate, adhesive coating exposed epoxy of divided chip, connecting chips
Patent Assignee: THIN FILM MODULE INC (THIN-N)
Inventor: HO C W
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20010016370	A1	20010823	US 99419512	A	19991018	200160 B
			US 2001846539	A	20010502	

Priority Applications (No Type Date): US 99419512 A 19991018; US 2001846539 A 20010502
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010016370	A1		13	H01L-021/44	Div ex application US 99419512

Abstract (Basic): US 20010016370 A1
Abstract (Basic):
NOVELTY - Epoxy layer is formed on surface A of substrate (14). Build-up multi-layer (BUM) on epoxy layer is exposed to form openings. Openings for **integrated circuit** (**IC**) chip are formed on surface B of substrate. Openings are created selectively in exposed epoxy. Substrate is subdivided, the exposed epoxy of chip is coated with adhesive, and chips are connected. Molding compound is applied on chips, and solder balls are inserted.
DETAILED DESCRIPTION - One or more **integrated circuit** (**IC**) chips having pads for electric connections are provided. A metal substrate (14) having first and second surfaces (24,26) is provided. The first surface of the metal substrate is cleaned and epoxy layer is deposited on the first surface of the substrate. An interconnect layer (20) is deposited on epoxy **layer** to form **first layer** of interconnect substrate (12). A build up multi-layer (BUM) is formed on the interconnect **layer** to form **second layer** of interconnect substrate. The BUM layer is coated with solder mask. The metal pads within BUM layer are exposed to create openings (32,33) for ball grid array (BGA) solder connections. The second surface of metal substrate is masked and etched to form one or more openings (28) for insertion of the **IC** chips. The portions of epoxy are exposed further within the openings. Openings are selectively created in exposed epoxy to provide electrical access and heat removal to interconnect substrate. The metal substrate is subdivided into individual **IC** chip substrates. The exposed epoxy

of individual **IC** chip substrate is coated with adhesive layer (17) for **wire bond** die. The adhesive is not required for flip **chip** die. **One** or more **IC chips** are inserted into **one** or more openings in individual **IC chips** substrates. A **wire bonded IC chip** is provided on adhesive coating. The **IC** chips are electrically connected through selectively created openings in epoxy by **wire bond** or reflow solder for flip chip case. A molding compound (22) is applied on **IC** chips. Solder balls (10,11) are inserted and attached to BGA solder connections.

INDEPENDENT CLAIMS are also included for the following:

(i) a structure for mounting one or more **integrated circuit** chips within a metal substrate; and

(ii) an interconnect structure comprising **one** or more insulating **films** and **one** or more conductive patterns.

The insulating films comprise epoxy material which is deposited or laminated on the substrate which is subsequently removed in part. The insulation film is used in suspension or in decal mode.

USE - For **mounting IC chips** such as **wire bond** and flip **chip** within metal substrate (claimed) for producing printed circuit boards which are used in the manufacture of large semiconductor functional units.

ADVANTAGE - Inexpensive and reliable method of high-density **wire bond** and flip **chip** semiconductor device manufacture is provided. The **wire bond** and flip **chip** device package significantly improves the cooling of mounted **IC** device. High pin fan-out for **wire bond** and flip **chip** semiconductor devices, is provided. The need for counter-balancing the effects of thick layers of dielectric for semiconductor device manufacture, is eliminated. The high density **wire bond** and flip **chip** semiconductor devices are packaged using BUM technology in combination with thin film deposition techniques. The high-density **wire bond** and flip **chip** semiconductor structures have good planarity initial surfaces. High-density **wire bond** and flip **chip** semiconductor structures are easily formed from structure devoid of warpage and dimensional variations by high temperature or wet chemical processing. A new method for mounting high-density **wire bond** semiconductor device is provided. The low cost, wide availability and versatility epoxy has thermal coefficient of expansion (TCE) higher than that of the metal substrate. The film which is present in the bottom of the cavity is stretched taut, and the film absorbs little water to provide a stable surface that does not sag or deform.

DESCRIPTION OF DRAWING(S) - The figure shows a single **chip wire bond chip** package to interconnect layers.

Solder balls (10,11)
Interconnect substrate (12)
Metal substrate (14)
Adhesive layer (17)
Interconnect layer (20)
Molding compound (22)
First and second substrates (24,26)
Openings (28)
Openings for BGA solder connections (32,33)

49/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013137919
WPI Acc No: 2000-309791/200027
XRPX Acc No: N00-232309
Manufacturing method for semiconductor package of **integrated circuit**, large-scale **integration**
Patent Assignee: KITASHIRO T (KITA-I)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000091364	A	20000331	JP 98253629	A	1998090	200027	B

Priority Applications (No Type Date): JP 98253629 A 19980908
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000091364	A		6	H01L-021/56	

Abstract (Basic): JP 2000091364 A
Abstract (Basic):
NOVELTY - A **first**-order resin **layer** (18) is coated between the outer lead (16) of a lead pin (13) and an inner lead (14). A plating process is applied to an inner island (11) and the inner **lead** of the **first**-order resin **layer**. The **wire bonding** of a semiconductor **chip** (12), **mounted** on the inner island, and the inner lead is performed. The inner island, the chip and the inner lead are sealed by a sealing body (17).

USE - For production of semiconductor package of **IC**, LSI.

ADVANTAGE - Enables simple manufacture of semiconductor package, since plating process can be performed easily without using special jig for partial plating. Does not need to use tap for restricting inner lead. Dam burr cutting becomes unnecessary after formation of sealing body, hence preventing damage of package.

DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of a semiconductor package.

Inner island (11)
Semiconductor chip (12)
Lead pin (13)
Inner lead (14)
Outer lead (16)
Sealing body (17)
First-order resin **layer** (18)
pp; 6 DwgNo 1/9

49/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012162353
WPI Acc No: 1998-579265/199849
XRAM Acc No: C98-173485
XRPX Acc No: N98-452006
Oxidation coating formation method for lead **frame** used in **IC mounting** - involves forming surface treatment layer consisting of oxidation coating, on surface of **lead frame** excluding other **two** surface treatment **layers**
Patent Assignee: MITSUI HIGH TEC KK (MIHI)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10261749	A	19980929	JP 9785838	A	19970319	199849	B

Priority Applications (No Type Date): JP 9785838 A 19970319
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10261749	A		5	H01L-023/50	

Abstract (Basic): JP 10261749 A

The method involves forming a surface treatment layer (25) consisting of Au or Ag with thickness 0.1-0.3micrometers on the **wire bonding** area of an element mounting portion (11) of a lead frame (14). Another surface treatment layer (26) consisting of Au plating layer with thickness 0.1-0.3micrometer is formed on the outer lead of lead frame. A surface treatment layer (27) consisting of oxidation coating is formed on the surface of the lead frame excluding the surface treatment layer (25,26).

ADVANTAGE - Avoids crack generation and peeling of sealing resin. Prevents diffusion of rust. Raises corrosion resistance nature of lead frame.

Dwg.1/3

49/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010880080
WPI Acc No: 1996-377031/199638
XRPX Acc No: N96-317614
Package for mounting semiconductor **IC** - has ground wiring which **connects first layer** substrate with metallic pattern of **chip** fixing hole of **second layer** substrate
Patent Assignee: OKI ELECTRIC IND CO LTD (OKID)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8181271	A	19960712	JP 94321997	A	19941226	199638	B

Priority Applications (No Type Date): JP 94321997 A 19941226
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8181271	A		9	H01L-023/50	

Abstract (Basic): JP 8181271 A

The package has a **second layer** substrate (12) which is laminated on a **first layer** substrate made of metal. The central part of the **first layer** substrate has a chip fixing part where as the **second layer** substrate has a chip fixing hole. Multiple wirings lines and a ground wiring (14) of a semiconductor chip are bonded to the upper surface of the **second layer** substrate by a **bonding wire**.

The ground wiring is arranged on the upper surface of the **second layer** substrate between the wiring signal and an end hole of the semiconductor chip fixing part. The ground wiring **connects** the **first layer** substrate with the metallic pattern of the chip fixing hole of the **second layer** substrate.

ADVANTAGE - Stabilises high frequency characteristics of **IC** at time of **chip mounting**. Improves performance at time of high speed operation of **IC**.

Dwg.1/15

49/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008353460
WPI Acc No: 1990-240461/199032
XRPX Acc No: N90-186608
Semiconductor device package pref. of DIP-type - has large- and small-current semiconductor chips included in single package to realise high integration packaging
Patent Assignee: TOSHIBA KK (TOKE)
Inventor: SAWAYA H
Number of Countries: 006 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 381054	A	19900808	EP 90101489	A	19900125	199032	B
JP 2201949	A	19900810	JP 8920219	A	19890130	199038	
US 5093713	A	19920303	US 91700301	A	19910508	199212	
EP 381054	A3	19930331	EP 90101489	A	19900125	199350	
KR 9309012	B1	19930918	KR 901013	A	19900130	199436	

Priority Applications (No Type Date): JP 8920212 A 19890130; JP 8920219 A 19890130
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 381054	A				
Designated States (Regional): DE FR GB					
US 5093713	A		5		
KR 9309012	B1			H01L-023/52	

Abstract (Basic): EP 381054 A
The semiconductor device package comprises a semiconductor chip (2), a substrate island region (1) for **mounting** the **chip** (2) and a lead frame (4) to serve as an external terminal of the chip (2), and including an island region (8) for mounting at least **one second** semiconductor **chip** (5). The substrate island region (1) constitutes a heat-radiation fin. The **first** semiconductor **chip** (2) comprises a large-current **chip** and the **second chip** (5) comprises a small-current chip.
The device further comprises a solder layer (3) for fixing the **first** semiconductor **chip** (2) to the substrate island region (1). A resin **layer** (7) insulates the **two** semiconductor **chips** (2,5). A **bonding wire** (6) electrically connects the **two chips** (2,5).
USE - Can be applied to single-in-line package or surface mount technical type package. (5pp Dwg.No.2/2
Abstract (Equivalent): US 5093713 A
The resin-sealed semiconductor device package has a semiconductor chip and a substrate island region for **mounting** the **first** semiconductor **chip**. A **lead** frame is arranged to serve as an external terminal of the **first** semiconductor **chip**, and includes an island region for mounting at least **one second** semiconductor **chip**. A resin layer thermally and electrically

insulates the **second** semiconductor **chip** from the **first** semiconductor **chip**. ADVANTAGE - Prevents abnormal heating of **IC**.
(5pp

49/3,AB/7 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06866543
SEMICONDUCTOR DEVICE

PUB. NO.: 2001-094046 [JP 2001094046 A]
PUBLISHED: April 06, 2001 (20010406)
INVENTOR(s): KOMIYAMA TADASHI
APPLICANT(s): SEIKO EPSON CORP
APPL. NO.: 11-269389 [JP 99269389]
FILED: September 22, 1999 (19990922)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a highly reliable semiconductor device that can retain stuck opposing surfaces between lamination **IC chips** in a **stacked** -type CSP essentially in parallel and can easily control insulation **film** thickness.

SOLUTION: **Two IC chips** 11 and 12 are mounted on the main surface of a base substrate 10 close to a chip size, while being laminated. An external terminal 13, such as a solder ball, is provided on the reverse side of the base substrate 10. Electrode pads 111 and 121 of the lamination **IC** chips 11 and 12 on the main surface of the base substrate 10, and the base substrate 10 are appropriately connected electrically with a **bonding wire** (gold **wire**) 14. An insulation support member 151 is included, at least at a periphery in an opposing region for sticking the **first** and **second IC chips** 11 and 12, and both the chips 11 and 12 are supported essentially in parallel.

49/3,AB/8 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

04928535
THREE-DIMENSIONAL BARE **CHIP** **IC** OF **TWO-LAYER** STRUCTURE

PUB. NO.: 07-221135 [JP 7221135 A]
PUBLISHED: August 18, 1995 (19950818)
INVENTOR(s): OKAYAMA AKITOSHI
APPLICANT(s): SUMITOMO ELECTRIC IND LTD [000213] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-033053 [JP 9433053]
FILED: February 03, 1994 (19940203)

ABSTRACT

PURPOSE: To obtain a three-dimensional bare chip **IC** having a structure, wherein a signal delay is made smallest, the **mounting** density of bare **chips** can be more enhanced in a optimum structure for a high-speed response element and a mounting operation is easy, by a method wherein the **two** bare **chips** are bonded together in opposition to each other using conductor bumps and moreover, the rear of the **chip** on **one** side of the **chips** is die-bonded on a substrate and the like.

CONSTITUTION: Chip electrode pads 13 and 14 are respectively formed on the surfaces of **two** semiconductor bare **chips** in such a way that the pads 13 and 14 are arranged in such an arrangement that when the chip 2 is turned over, the pads 14 and 13 coincide with each other and the fellow chip electrode pads 13 and 1 4 are bonded together using conductor bumps 4. The rear of the **chip** 1 on **one** side of the **chips** 1 and 2 is die-bonded on carriers, such as a substrate 7, a lead frame and a package, and electrode pads 10 on the chip 1 with the rear bonded on the carriers and pads 6 on the electrode 7 are **bonded** together by **wire bonding** . For example, bumps 4 are respectively formed on pads 13 on a **first chip** 1, a **second chip** 2 is put on the **first chip** 1 by turning the chip 2 over to make the fellow pads 13 and pads 14, oppose to each other and the **two** **chips** are bonded together by thermol compression bonding.

49/3,AB/9 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

03880387
OPTICAL SIGNAL MODULE

PUB. NO.: 04-245487 [JP 4245487 A]
PUBLISHED: September 02, 1992 (19920902)
INVENTOR(s): WADA YOSHIYUKI
YUZUHARA KAZUNORI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
KIYUUSHIYUU DENSHI KK [000000] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-010460 [JP 9110460]
FILED: January 31, 1991 (19910131)
JOURNAL: Section: E, Section No. 1305, Vol. 17, No. 15, Pg. 62, January 12, 1993 (19930112)

ABSTRACT

PURPOSE: To reduce the size of an optical signal module by a method wherein the module is provided with **two lead frames**, which are respectively arranged on **two layers** and are a lead **frame** for optical semiconductor **mounting** use and a **lead frame** for **mounting** a semiconductor **chip** constituting a peripheral circuit.

CONSTITUTION: **Two lead frames** 6 and 7 are respectively arranged on **two** upper and lower **layers**, an optical semiconductor element 1, such as a light- emitting diode, a photodetecting diode or the like, is mounted on the upper side lead frame 6, a semiconductor chip 2, which is an **integrated circuit** constituting a peripheral circuit, such as a drive circuit, a photodetecting signal processing circuit or the like, is mounted on the lower side lead frame 7 and after being electrically connected to each other via **bonding wires** 5, the **lead frames** are encapsulated in a case 3 which is a transparent resin mold. Thereby, a reduction in the size of an optical signal module becomes possible and at the same time, the erroneous operation of the module, which is caused by an effect to the peripheral circuit due to an optical signal of the element 1, can be suppressed.

49/3,AB/10 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

03522853
MANUFACTURE OF HYBRID **INTEGRATED CIRCUIT**

PUB. NO.: 03-185753 [JP 3185753 A]
PUBLISHED: August 13, 1991 (19910813)
INVENTOR(s): NAKAJIMA TAKESHI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-325134 [JP 89325134]
FILED: December 14, 1989 (19891214)
JOURNAL: Section: E, Section No. 1131, Vol. 15, No. 442, Pg. 22, November 11, 1991 (19911111)

ABSTRACT

PURPOSE: To efficiently use materials and to enhance economical efficiency by a method wherein, even when a semiconductor **IC** chip malfunctions, the other materials including a substrate are utilized.

CONSTITUTION: Ag paste 2 is printed on a ceramic substrate 1, and an **IC chip** 3 is **mounted** thereon. The Ag paste is solidified by conducting a curing operation under the above-mentioned state. Then, a **bonding wire** 4 is connected. An interim characteristic inspection is conducted under the above-mentioned state, and if the inspected chip is judged as a non-defective **one**, it is **coated** with precoating resin 5 and sent to the next process. Also, when the chip is judged as a defective **one**, another **IC chip** 7 is **mounted** after Ag paste 6 has been printed. As a result, the substrate 1, having a high ratio of materials cost, and other parts can economically be used.

49/3,AB/11 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

03387860
LEAD FRAME FOR MOLD **IC**

PUB. NO.: 03-050760 [JP 3050760 A]
PUBLISHED: March 05, 1991 (19910305)
INVENTOR(s): YOKOSUKA SHIGERU
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-186703 [JP 89186703]
FILED: July 18, 1989 (19890718)
JOURNAL: Section: E, Section No. 1068, Vol. 15, No. 191, Pg. 106, May 16, 1991 (19910516)

ABSTRACT

PURPOSE: To prevent separation of mold resin from a lead frame by constituting the **lead frame** of a **first** heat-resistant resin **layer** , an island composed of metal film and a plurality of leads formed on the resin **layer**, and a **second** heat- resistant resin having apertures on the island and at the opposite ends of the lead.

CONSTITUTION: A lead frame 10 is constituted of the following; plane type heat-resistant resin 11A, an island 4 composed of copper foil and a plurality of leads 1 formed on the resin 11A, and heat-resistant resin 11B in the upper layer having aperture parts on the island 4, the outer connection parts 2 of the leads 1 and on bonding parts 3. Notches 8 are made in the under side of the heat-resistant resin of the lead frame 10. When a mold **IC** is manufactured using the lead frame 10, a semiconductor **chip** 6 is **mounted** on an island 4, a pad of the semiconductor chip 6 and the bonding part 3 of the lead 1 are **jointed** through a **bonding wire** 7. After that, resin sealing is performed with mold resin 5, with the lead frame 10 being bent at the parts of the notches 8. By such arrangement, separation of the mold resin from the lead is prevented, and moisture resistance can be improved.

49/3,AB/12 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

02706436
FLEXIBLE WIRING BOARD AND **WIRE BONDING**

PUB. NO.: 01-004036 [JP 1004036 A]
PUBLISHED: January 09, 1989 (19890109)
INVENTOR(s): OGAWA NAOAKI
TANAKA YOSHITAKA
UCHIBORI TOYOICHI
APPLICANT(s): MITSUI MINING & SMELTING CO LTD [000618] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-158936 [JP 87158936]
FILED: June 26, 1987 (19870626)
JOURNAL: Section: E, Section No. 748, Vol. 13, No. 173, Pg. 94, April 24, 1989 (19890424)

ABSTRACT

PURPOSE: To obtain a uniformly and firmly bonded part by a method wherein a metal layer is formed at a **mounting** part and a **lead** part on the surface to be **wire-bonded** via an insulating layer.

CONSTITUTION: **Two** or more **lead** patterns 3 directed toward an **IC** pad 2 are formed on the surface of a wiring board 1; **one** square copper **layer** is formed on the rear. A cross section of a line A-A is composed of the lead patterns 3, an adhesive agent layer 5a, a polyimide layer 6a, an adhesive agent layer 5b, a copper layer 4, an adhesive agent layer 5c and a polyimide layer 6c. An **IC chip** is **wire-bonded** by an ultrasonic welding method. Because the copper layer is formed on the rear, the **wire bonding** performance is enhanced. Especially when an ultrasonic vibration is perpendicular to the lead patterns, the performance is enhanced remarkably.

49/3,AB/13 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO

01701654
SEMICONDUCTOR DEVICE

PUB. NO.: 60-180154 [JP 60180154 A]
PUBLISHED: September 13, 1985 (19850913)
INVENTOR(s): TAKISHIMA SHOJI
APPLICANT(s): CLARION CO LTD [325708] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-035837 [JP 8435837]
FILED: February 27, 1984 (19840227)
JOURNAL: Section: E, Section No. 376, Vol. 10, No. 20, Pg. 44, January 25, 1986 (19860125)

ABSTRACT

PURPOSE: To realize a package having high density by forming a lead frame in multilayer structure, in which a plurality of conductive layers are insulated mutually, and **wire-bonding** each conductive layer and different electrodes on a semiconductor element.

CONSTITUTION: A lead frame is formed in multilayer structure in which sections among **first** conductor **layers** 15 and **second** conductor **layers** 16 are insulated electrically by insulating layers 17. Sections among the end sections 15A of the **first** conductive **layers** 15 in several external lead 11 and the end sections 16A of the **second** conductive **layers** 16 and different electrodes 18 on an **IC** chip 14 are **bonded** by **wires** 19, the electrodes 18 on the **IC** chip 14 are lead out electrically to the outside, a desired section is molded by a resin, and sections among external leads are isolated electrically, thus completing a semiconductor device. Accordingly, the same result as **two** external **leads** are **wire-bonded** is obtained in **one** external **lead**, and the **mounting** density of a package can be doubled

51/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014582517
WPI Acc No: 2002-403221/200243
XRAM Acc No: C02-113350
XRPX Acc No: N02-316335
Stacked semiconductor device comprises first and second substrates, first and second terminals, and at least one **first** and **second** semiconductor **chips**
Patent Assignee: FUJITSU LTD (FUIT)
Inventor: AKASHI Y; ANDO F; IKEDA M; KIKUMA K; NISHIMURA T; OKUDA H; ONODERA H; OZAWA K; TAKASHIMA A; TSUKIDATE Y; UNO T
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020027295	A1	20020307	US 2001940625	A	20010829	200243	B
JP 2002151644	A	20020524	JP 2001121539	A	20010419	200250	

Priority Applications (No Type Date): JP 2001121539 A 20010419; JP 2000267621 A 20000904
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020027295	A1		39	H01L-023/48	
JP 2002151644	A		25	H01L-025/065	

Abstract (Basic): US 20020027295 A1
Abstract (Basic):
NOVELTY - Stacked semiconductor device comprises a first substrate having external connecting terminals; first terminals on first substrate surface; at least **one first** semiconductor **chip** on **first** substrate; a second substrate on **first** semiconductor **chip**; at least **one second** semiconductor **chip** on **second** substrate; and second terminals formed on second substrate.
DETAILED DESCRIPTION - A stacked semiconductor device comprises a first substrate that has external connecting terminals; first terminals that are placed on a surface of the first substrate opposite to a surface of the first substrate on which the external connecting terminals of the first substrate are formed; at least **one first** semiconductor **chip** (22) that is **mounted** on the first substrate; a second substrate that is placed on the **first** semiconductor **chip**; at least **one second** semiconductor **chip** (24) that is **mounted** on the second substrate; and second terminals that are formed on the second substrate and electrically connected to at least one of the **first** semiconductor **chip** and the **second** semiconductor **chip**. The **second** terminals are connected to the first terminals by **wire bonding**. An INDEPENDENT CLAIM is also included for a method of producing a stacked semiconductor device, which comprises:
(a) forming protruding electrodes on a **first** semiconductor **chip**;

(b) **mounting** the **first** semiconductor **chip** on a **second** substrate by flip-**chip** bonding;

(c) securing a **second** semiconductor **chip**, which is smaller than the second substrate, to a side of the second substrate opposite to a side on which the **first** semiconductor **chip** is **mounted**, and securing the **first** semiconductor **chip** to a front surface of a first substrate;

(d) connecting the **first** and **second** semiconductor **chips** to the **first** substrate by **wire bonding**;

(e) encapsulating the **first** and **second** semiconductor **chips** and the **second** substrate on the first substrate; and

(f) forming external connecting electrodes on a back surface of the first substrate.

USE - As stacked semiconductor device.

ADVANTAGE - The stacked semiconductor device allows semiconductor chips of desired sizes to be stacked as one package.

DESCRIPTION OF DRAWING(S) - The drawing shows a sectional view of a part of a stacked semiconductor device.

semiconductor chips (22,24)

flexible printed wiring board (26)

pp; 39 DwgNo 3/27

51/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009796162
WPI Acc No: 1994-076015/199410
XRPX Acc No: N94-059406
Semiconductor device with controlled input current to semiconductor chip for output current supply - has conductive **layers** on **two** different composite insulating substrates so that input and output current paths are in reverse directions, with semiconductor power element and one substrate mounted on second substrate
Patent Assignee: MITSUBISHI DENKI KK (MITQ); MITSUBISHI ELECTRIC CORP (MITQ); MITSUBISHI ELECTRIC KK (MITQ)
Inventor: ARAI K; TAKAGI Y
Number of Countries: 006 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 585578	A1	19940309	EP 93111381	A	19930715	199410	B
JP 6045509	A	19940218	JP 92193979	A	19920721	199412	
US 5424579	A	19950613	US 9384957	A	19930702	199529	
EP 585578	B1	19970312	EP 93111381	A	19930715	199715	
DE 69308691	E	19970417	DE 608691	A	19930715	199721	
			EP 93111381	A	19930715		
KR 120918	B1	19971020	KR 9311287	A	19930621	199948	

Priority Applications (No Type Date): JP 92193979 A 19920721
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 585578	A1	E	25	H01L-023/64	
Designated States (Regional): DE FR GB					
US 5424579	A		18	H01L-023/02	
EP 585578	B1	E	27	H01L-023/64	
Designated States (Regional): DE FR GB					
DE 69308691	E			H01L-023/64	Based on patent EP 585578
JP 6045509	A			H01L-023/60	
KR 120918	B1			H01L-027/04	

Abstract (Basic): EP 585578 A
The semiconductor device includes an insulating substrate on a metal baseplate. There is a conductive layer e.g. a copper pattern deposited on the insulating substrate which, in one area, conducts either the input or output current parallel to the baseplate surface. A second composite insulating substrate (9) is selectively mounted on the conductive layer, and has a conductive layer e.g. a coper pattern region which, in one area, conducts the other of the input or output current in a direction antiparallel to the first current direction in the first composite substrate.
A semiconductor **chip** is **mounted** on **one** conductive **layer** and is **connected** electrically to both conductive layers e.g. by **wire bonds** (13). Pref. the semiconductor chip includes a power semiconductor element e.g. IGBT connected to a flywheel diode, both on the **first** conductive **layer**. There

may be a conductive layer e.g. of copper between the baseplate and the first insulating substrate.

USE/ADVANTAGE - Power module. Increased switching frequency in ON to OFF operation does not increase surge voltage, due to reduced floating inductance; avoids device breakdown.

Dwg.3/17

Abstract (Equivalent): EP 585578 B

A semiconductor device for controlling an input current by a semiconductor chip to provide an output current, comprising: (a) a metal base plate (1) having a major surface; (b) a first insulating substrate (3) disposed on said major surface of said metal base plate; (c) a **first** conductive **layer** (4) provided on said first insulating substrate and having (c-1) a first region (4a) for conducting one of said input and output currents in a first direction (X) parallel to said major surface, and (c-2) a second peninsular region (4b, 4c) continuous with said first region and protruding therefrom in a second direction (Y) different from said first direction (X) on said major surface; (d) a second insulating substrate (7) provided on said **first** conductive **layer** (4) except at least an end portion of said second region (4b, 4c); (e) a **second** conductive **layer** (8) provided on said second insulating substrate (7) and having a third region (8a) for conducting the other current in a third direction antiparallel to said first direction, said third region (8a) overlaying said first region (4a) of said **first** conductive **layer** (4); and (f) at least **one** semiconductor **chip** (12) provided on said second region (4b, 4c) or said **second** conductive **layer** (8) and **connected** electrically to said second region (4b, 4c) and said **second** conductive **layer**.

Dwg.1/17

Abstract (Equivalent): US 5424579 A

The semiconductor device includes an insulating substrate on a metal baseplate. There is a conductive layer e.g. a copper pattern deposited on the insulating substrate which, in one area, conducts either the input or output current parallel to the baseplate surface. A second composite insulating substrate (9) is selectively mounted on the conductive layer, and has a conductive layer e.g. a coper pattern region which, in one area, conducts the other of the input or output current in a direction antiparallel to the first current direction in the first composite substrate.

A semiconductor **chip** is **mounted** on **one** conductive **layer** and is **connected** electrically to both conductive layers e.g. by **wire bonds** (13). Pref. the semiconductor chip includes a power semiconductor element e.g. IGBT connected to a flywheel diode, both on the **first** conductive **layer**. There may be a conductive layer e.g. of copper between the baseplate and the first insulating substrate.

USE/ADVANTAGE - Power module. Increased switching frequency in ON to OFF operation does not increase surge voltage, due to reduced floating inductance; avoids device breakdown.

Dwg.1/17

51/3,AB/3 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

05183956
MANUFACTURING METHOD OF SEMICONDUCTOR MOUNTING MULTI-LAYER WIRING BOARD

PUB. NO.: 08-139456 [JP 8139456 A]
PUBLISHED: May 31, 1996 (19960531)
INVENTOR(s): ISONO MASASHI
MIMORI SEIJI
ASAKAWA TORU
NAKAMURA MASANORI
APPLICANT(s): HITACHI CHEM CO LTD [000445] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-276510 [JP 94276510]
FILED: November 10, 1994 (19941110)

ABSTRACT

PURPOSE: To form a cavity for efficiently mounting semiconductor having excellent freedom in design by a method wherein, after the formation of an aperture part by back facing step, etc., an outer layer circuit is formed using an Au plating as an etching resist on the outermost second substrate electrolessly copper-plated.

CONSTITUTION: The first substrate 3 having an aperture part for **mounting** a semiconductor **chip**, the **first** insulating **layer** 2 and the **second** substrate 1 are successively laminated above the substrate 3 while the **second** insulating **layer** 4 and the third substrate 5 are successively laminated below the substrate 3 to be **thermoset** for laminated integration. Next, a through hole is made to copper plate 7 the hole inner wall and the surface electrolessly. Next, another aperture part is formed on the outermost second substrate 1 by back facing step. Later, a resist 8 for Au plating is formed to perform nickel plating and a **wire bonding** part is Au-plated 9, prospected outer layer circuit and a copper film surface inside the through hole. Finally, after peeling the resist for Au plating, the copper layer is etched away to form the outer layer circuit.

51/3,AB/4 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

03878056
PLASTIC PGA PACKAGE

PUB. NO.: 04-243156 [JP 4243156 A]
PUBLISHED: August 31, 1992 (19920831)
INVENTOR(s): IKA MASAO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-003562 [JP 913562]
FILED: January 17, 1991 (19910117)
JOURNAL: Section: E, Section No. 1304, Vol. 17, No. 13, Pg. 98, January 11, 1993 (19930111)

ABSTRACT

PURPOSE: To cause the title package to correspond to a small pad pitch by arranging front-row and rear-row bonding leads zigzag on the surface of a plastic substrate and by arranging wires from said front-row bonding leads in the manner of passing the wires between the two front-row and rear-row bonding leads.

CONSTITUTION: The bonding leads of a package are arranged in two rows and the front-row and rear-row bonding **leads** out of the **two** rows are arranged zigzag. Wires 1a in package from the front-row bonding leads 1 are narrower in width than the front-row bonding leads 1 and arranged between the front-row and rear-row bonding leads 1 and 2. A **chip** 3 is **mounted** in a cavity 4 called an island and pads 6 on the chip and the bonding leads are electrically connected by **bonding wires** 5. Thus, it is possible to realize bonding similar to ceramic PGA having **two layers** or more of wires in package.

51/3,AB/5 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

03273756
SEMICONDUCTOR DEVICE

PUB. NO.: 02-249256 [JP 2249256 A]
PUBLISHED: October 05, 1990 (19901005)
INVENTOR(s): ITO KIYOSHI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-278856 [JP 88278856]
FILED: November 02, 1988 (19881102)
JOURNAL: Section: E, Section No. 1015, Vol. 14, No. 573, Pg. 124, December 19, 1990 (19901219)

ABSTRACT

PURPOSE: To absorb an instantaneous surge voltage generated by a human body, production equipment, etc., and protect a semiconductor chip from application of a high voltage by a method wherein the bottom electrode of the semiconductor **chip** is **mounted** on a dielectric heatsink attached to a mounting post and the heatsink is provided electrically in parallel with the semiconductor chip.

CONSTITUTION: A package 4 which has a **first lead** 4c jointed to the bottom of a conductive base 4b, a **second lead** 4d which is inserted into a through-hole drilled in the base 4b and isolated from and fixed to the base 4b with insulating sealing glass 7 and a mounting post 4a provided on the base 4b, a dielectric heatsink 2 attached to the mounting post 4a, a conductor layer 3a provided on the surface of the heatsink 2 opposite to the mounting post 4a, a semiconductor chip 1 whose bottom electrode is mounted on the conductor **layer** 2a, a **first bonding wire** 3a with which the upper electrode of the semiconductor chip 1 is connected to the mounting post 4a and a second **bonding wire** 3b with which the conductor **layer** 2a is **connected** to the **second lead** 4d are prov

53/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014268692
WPI Acc No: 2002-089390/200212
XRAM Acc No: C02-027495
XRPX Acc No: N02-065886
Leadframe for assembly of **integrated circuit** chips comprises a base metal structure having a nickel layer, lead-free solder layer on the nickel **layer** for parts **attachment** and palladium **layer** on the nickel **layer** for **bonding wire attachment**
Patent Assignee: ABBOTT D C (ABBO-I)
Inventor: ABBOTT D C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20010054750	A1	20011227	US 2000214314	P	20000627	200212 B
			US 2001887857	A	20010622	

Priority Applications (No Type Date): US 2000214314 P 20000627; US 2001887857 A 20010622
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010054750	A1		12	H01L-023/495	Provisional application US 2000214314

Abstract (Basic): US 20010054750 A1
Abstract (Basic):
NOVELTY - Leadframe comprises: a base metal structure having an adherent layer comprising nickel covering the base metal; an adherent layer of lead-free solder on the nickel layer, selectively covering areas of the leadframe suitable for parts **attachment**; and an adherent **layer** comprising palladium on the nickel layer, selectively covering areas of the leadframe suitable for **bonding wire** attachment.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of forming a leadframe structure comprising a **chip mount** pad (35) and a number of lead segments (33), each having a first end near mount pad and a second end remote from the mount pad. The method comprises:
(a) forming the structure from a sheet-like starting material;
(b) plating a nickel layer on the leadframe;
(c) selectively masking the **chip** pad and the **first** segment ends, thereby leaving the second segment ends exposed;
(d) plating a lead-free solder layer onto the nickel layer on the exposed segment ends in a thickness suitable for parts attachment;
(e) selectively masking the second segment ends, thereby leaving the **chip** pad and the **first** segment ends exposed; and
(f) plating a palladium layer on the nickel layer on the exposed chip pad and segment ends in a thickness suitable for **bonding wire** attachment.
USE - The leadframe is used in the assembly of **integrated**

circuit chips (claimed).

ADVANTAGE - The leadframe can be mass produced at low cost. The leadframe functions are maximized. The solder spot-plated copper leadframe provides for easy and reliable solder attachment to boards or other parts of the formed leadframe segments. Environmental protection and assembly flexibility of semiconductor packages are enhanced.

DESCRIPTION OF DRAWING(S) - The drawing shows a simplified top view of an example of a leadframe unit for semiconductor devices.

Carrier rail (30)
Outer leadframe (31)
Lead segments (33)
Chip mount pad (35)
Support members (36)
Dam bar (37)
Pilot holes (38)
pp; 12 DwgNo 3/6

53/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004081709
WPI Acc No: 1984-227250/198437
XRAM Acc No: C84-095801
XRPX Acc No: N84-169828
Semiconductor chip carrier and contact array package - includes a heat sink insert contacting the chip in a recessed chip **connection layer**
Patent Assignee: PRINTED CIRCUITS INT (PRIN-N)
Inventor: MILLER T J; STENERSON G L
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2136205	A	19840912	GB 845827	A	19840306	198437	B
JP 59201449	A	19841115	JP 8443026	A	19840308	198501	
US 4630172	A	19861216	US 83473482	A	19830309	198701	

Priority Applications (No Type Date): US 83473482 A 19830309
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2136205	A		11		

Abstract (Basic): GB 2136205 A
Package comprises : a dielectric layer (I); an aperture in (I); a chip **connection layer** (II) bonded to the surface of (I); a chip holding recess in (II); a heat-conducting base extending across the aperture below (II) and extending across the recess so that it is in heat-conducting contact with the **chip mounted** in the recess; and a contact array outboard of the recess extending from (II).

ADVANTAGE - Device has good heat dissipation for high power 12s.
0/8

Abstract (Equivalent): US 4630172 A
Semiconductor chip carrier and contact array package has an apertured dielectric bottom **layer** (11) and chip **connection layers** (16,17) insulated from each other. There is at least **one chip**-holding recess (24) in the **wire bond** layers and a heat conductive Cu heat sink insert (26) across the aperture of the dielectric layer and forming a base in contact with the bottom of an **integrated circuit** chip (27). Metallisation patterns (29) in the **wire bond** layers (16,17) bond the chip and a grid of connection pins (20) is connected to plated holes in the **wire bond** layers.
ADVANTAGE - Reliable compact structure with high heat dissipation properties.
(10pp

53/3,AB/3 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06386708
IC MODULE FOR **IC** CARD

PUB. NO.: 11-328355 [JP 11328355 A]
PUBLISHED: November 30, 1999 (19991130)
INVENTOR(s): TSUCHIYA NORIO
APPLICANT(s): DAINIPPON PRINTING CO LTD
APPL. NO.: 10-153683 [JP 98153683]
FILED: May 20, 1998 (19980520)

ABSTRACT

PROBLEM TO BE SOLVED: To secure the joining of an **IC** module and to improve the manufacture yield of the **IC** card by providing a connecting means which projects acutely at the contact part where the **IC** module and an antenna terminal are connected together.

SOLUTION: The **IC** module 10 has a printed board 11 and an **IC chip** 12. On **one** surface of the printed board 11, an external contact terminal part 13 is provided and on the other surface of the printed board 11, a wiring pattern layer 14 is provided. The external connection terminal part 13 and wiring pattern **layer** 14 are **connected** electrically through a through hole 19. An **IC chip** is **mounted** on the printed board 11 on the side of the wiring pattern layer, and a die pad of the **IC** chip and the wiring pattern **layer** 14 are **connected** electrically by a **bonding wire** 18. This **IC** module has a joining means 15 which projects acutely onto the wiring pattern **layer** 14 **connecting** to the antenna. The joining means 15 is made of a conductive metal material or a resin material wherein conductive metal powder is dispersed.

53/3,AB/4 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

03098546
SEMICONDUCTOR **INTEGRATED CIRCUIT** DEVICE

PUB. NO.: 02-074046 [JP 2074046 A]
PUBLISHED: March 14, 1990 (19900314)
INVENTOR(s): IDENO MASAAKI
APPLICANT(s): NEC IC MICROCOMPUT SYST LTD [470861] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-225767 [JP 88225767]
FILED: September 09, 1988 (19880909)
JOURNAL: Section: E, Section No. 935, Vol. 14, No. 255, Pg. 35, May 31, 1990 (19900531)

ABSTRACT

PURPOSE: To eliminate an increase in the size of a case as well as to lessen the sizes of semiconductor **integrated circuit** chips and to contrive the improvement of a yield by a method wherein the semiconductor **integrated circuit** chips are placed in order on a case island in order of size.

CONSTITUTION: A **first integrated circuit chip** 1 is **mounted** on a case island 3 and a **second integrated circuit chip** 4 is fixed on the chip 1 in such a way that a conductive **film** 5 for external **connection** use of the chip 1 is exposed. Here, the film 5 of the chip 1 and a conductive **film** 6 for external **connection** use of the chip 4 are respectively connected with case **leads** 2 by **bonding wires** 7. Thereby, large scale circuits can be housed in the same case without enlarging the size of a case. Moreover, as there is no need to constitute a large scale circuit on **one chip**, the sizes of the **integrated circuit** chips are also reduced and the improvement of a yield can be contrived.

53/3,AB/5 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

02664549
MANUFACTURE OF LAMINATED SUBSTRATE FOR MOUNTING **INTEGRATED CIRCUIT**

PUB. NO.: 63-281449 [JP 63281449 A]
PUBLISHED: November 17, 1988 (19881117)
INVENTOR(s): TAKAHARA MASAYOSHI
APPLICANT(s): CLARION CO LTD [325708] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-117424 [JP 87117424]
FILED: May 13, 1987 (19870513)
JOURNAL: Section: E, Section No. 728, Vol. 13, No. 110, Pg. 24, March 16, 1989 (19890316)

ABSTRACT

PURPOSE: To inhibit the retention of chemicals used by a **chip mounting** process by fixing a second substrate, to which a hole section or a recessed section is formed, to a section **coating** the electrical **connecting** section of a **chip** fastened onto a **first** substrate, to which a pattern is shaped, and the pattern and bringing a printed substrate to a multilayer state.

CONSTITUTION: An **integrated circuit** mounting section 2 and circuit patterns 3 are shaped onto a substrate 1 as a base substrate, and the mounting section 2 is plated with a metal (Au, etc.). The whole is washed for removing an impurity such as remaining and adhering alkali metallic ions, halogen ions, etc., and the substrate is baked and an **integrated circuit** (a **chip**) 4 is **mounted** to the mounting section 2 by using paste such as an Au-Si eutectic, and **bonded** by **wires** 6. The **integrated circuit** mounting section and **wire bonding** sections are coated (bonding may be used) by employing a synthetic resin 7, and baked for curing the resin. The printed substrate 1 in which the circuit patterns are shaped and the **integrated circuit** is mounted completely is used as the base substrate, and other printed substrates are laminated onto the substrate 1 by employing adhesives such as the resin, thus forming a laminated substrate.

60/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004837728
WPI Acc No: 1986-341069/198652
XRPX Acc No: N86-254519
Packaging semiconductor device with heat sink - uses moulding layer sealing bed and sealing heat sink, **first layer** and sink-bed **gap**
Patent Assignee: TOSHIBA KK (TOKE)
Inventor: EMOTO T; KATO T; KOJIMA S; MATSUMOTO H
Number of Countries: 006 Number of Patents: 010
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 206771	A	19861230	EP 86304725	A	19860619	198652	B
JP 61292346	A	19861223	JP 85134658	A	19850620	198705	
JP 62076659	A	19870408	JP 85214852	A	19850930	198720	
JP 62229961	A	19871008	JP 8671134	A	19860331	198746	
US 4924351	A	19900508	US 89334771	A	19890410	199023	
KR 9001668	B	19900317				199105	
KR 9001833	B	19900324				199106	
KR 9001984	B	19900330				199106	
EP 206771	B	19920311	EP 86304725	A	19860619	199211	
DE 3684184	G	19920416				199217	

Priority Applications (No Type Date): JP 8671134 A 19860331; JP 85134658 A 19850620; JP 85214852 A 19850930
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 206771	A	E	23		
Designated States (Regional): DE FR GB					
EP 206771	B		12		
Designated States (Regional): DE FR GB					

Abstract (Basic): EP 206771 B
The moulded layer seals a semiconductor chip (4), a bed part (21), a set of bonding wires (6) and a heat sink (1) which has a **gap** of a prescribed distance between the heat sink (1) and the back of the bed part (21). The layer comprises a moulded layer (3a) which seals to expose the back of the bed part and a **second** moulded **layer** (3b) is formed to cover sides of the heat sink (1) and of the **first** moulded **layer** (3a).
The intermediate parts of the **leads** (2) are **coupled** to the **chip** via the bonding wires, and the **gap** is fulled between the bed part (21) and the heat sink (1). A part fo the **first layer** can be unfilled by a notch or through-hole.
ADVANTAGE - Prevents voids and allows increased silica content of resin layer. (23pp Dwg.No.8/11
Abstract (Equivalent): EP 206771 B
A method of manufacturing a packaged semiconductor device, said device comprising a bed part (21), a semiconductor **chip** (4) **mounted** on said bed part (21), leads (2) connected by bonding

wires (6) to the internal terminals of said semiconductor chip (4), a heat sink (1) disposed under a back of said bed part (21) and with a **gap** between said heat sink (10 and said back of said bed part (21), and a moulded layer which seals said semiconductor chip (4), bed part (21), bonding wires (6) end of said leads (2), and said heat sink (1), the method including: forming a **first** moulded **layer** (3a) to seal the bed part such that the back of the bed part (21) is exposed; leaving a reduced **gap** between said **first** moulded **layer** (3a) and said heat sink (1); forming a **second** moulded **layer** (3b) by **first** filling said reduced **gap** and then covering the sides of the heat sink (1) and the sides of the **first** moulded **layer**. (12pp)o

Abstract (Equivalent): US 4924351 A

The packaged semiconductor device includes a bed part having front and back surface. A semiconductor **chip** is **mounted** on the front surface. A moulded layer seals the front surface of the bed part and the semiconductor chip to expose the back surface. A heat sink faces the back surface of the bed part on a main surface with a **gap** of a prescribed distance from the back surface.

A **second** moulded **layer** is formed to cover an outside of the heat sink and the moulded layer and fills the **gap** from **one** direction. Leads pass through the **second** moulded **layer**, of which ends are disposed inside the **first** moulded **layer**, and which are **connected** to internal terminals of the semiconductor **chip**. At least **one** of the back surface of the bed part and the first main surface of the heat sink is provided with roughened recessed parts.

ADVANTAGE - Distance between bed part and heat sink shortened, generation of voids prevented, crystalline silica content of the moulded resin layer interposed between the bed part and the heat sink increased, and thermal dissipation characteristics improved without decreasing dielectric breakdown.

(9pp

62/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009870665
WPI Acc No: 1994-150566/199418
Related WPI Acc No: 1991-303225; 1992-150201; 1993-027130; 1993-235255
XRAM Acc No: C94-069249
XRPX Acc No: N94-118202
Semiconductor package with heat sink assembly - includes flat heat sink member mounted on top of circuit die through polyepoxy encapsulant
Patent Assignee: LSI LOGIC CORP (LSIL-N)
Inventor: FULCHER E; ROSTOKER M D; SCHNEIDER M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5311060	A	19940510	US 89454752	A	19891219	199418 B
			US 91671677	A	19910319	
			US 92865817	A	19920401	
			US 92922713	A	19920728	

Priority Applications (No Type Date): US 92922713 A 19920728; US 89454752 A 19891219; US 91671677 A 19910319; US 92865817 A 19920401
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5311060	A		12	H01L-039/02	Cont of application US 89454752 Cont of application US 91671677 CIP of application US 92865817 CIP of patent US 5175612

Abstract (Basic): US 5311060 A

Device comprises a die attach pad (50) on which a die (52) is **mounted**; **leads** (48) extending outward from adjacent the die attach pad; a **first** plastic **film** (44) formed on the leads, a portion bridging the **gap** between the lead inner ends and the pad, leaving a portion of the **leads** exposed; **bond wires** (54) connecting circuit elements on top of the die to the exposed portions of the **lead** inner ends; a **second** plastic **film** (46) formed beneath the leads and beneath the edge of the pad; a ring frame (56) on the leads; epoxy (94) on the leads completely encapsulating the die and extending to the ring frame; and an integral heat sink structure (82) on top of the die embedded in the epoxy and facing circuit elements via a passivation layer.

The heat sink has an upper portion (86) extending from within the epoxy to at least the exterior surface of the epoxy and ridged (92) for adhesion to the epoxy, and a lower portion (84) in contact with the passivation layer. The heat sink has a flat registration surface (87) onto which a second 'add-on' heat sink structure (96) can be added, pref. via a button fit or an epoxy bond.

ADVANTAGE - Heat sink structure provides improved heat dissipation esp. for thermal mass or air-cooled devices and can be easily assembled by automated techniques.

Dwg.3/4

66/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013852155
WPI Acc No: 2001-336368/200136
XRPX Acc No: N01-242802
Semiconductor device including several semiconductor **chips** has **second** semiconductor **chip** and **multilayered** printed circuit board **connected** electrically and sealed by resin to fill out **gap** between them
Patent Assignee: FUJITSU MEDIA DEVICES LTD (FUJI-N); SHINKO DENKI KOGYO KK (SHIA)
Inventor: TAKEDA H
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 10009733	A1	20001012	DE 1009733	A	20000302	200136	B
JP 2000269408	A	20000929	JP 9969013	A	19990315	200136	
US 6414381	B1	20020702	US 2000495699	A	20000201	200248	

Priority Applications (No Type Date): JP 9969013 A 19990315
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 10009733	A1		16	H01L-025/065	
JP 2000269408	A		12	H01L-025/065	
US 6414381	B1			H01L-023/495	

Abstract (Basic): DE 10009733 A1
Abstract (Basic):
NOVELTY - An intermediate link holds over first (22A) and **second** semiconductor **chip** (22B) in such a way that between the **first** semiconductor **chip** (22A) and the **second** semiconductor **chip** (22B) a **gap** is formed. The **second** semiconductor **chip** (22B) and the multilayered printed circuit board (23) are connected electrically and sealed by a resin (25) to fill out the **gap** between them.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for:
(a) a method for producing of a semiconductor device
USE - For producing a semiconductor device with a several of semiconductor **chips** in a **stack** structure.
ADVANTAGE - Reduced size and improved assembly reliability in which multi-purpose semiconductor chips can be used.
DESCRIPTION OF DRAWING(S) - The drawing shows a first embodiment of the semiconductor device according to a first embodiment of the present invention.
first semiconductor **chip** (22A)
second semiconductor **chip** (22B)
multilayered printed circuit board (23)
resin (25)
pp; 16 DwgNo 5/10

66/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011956526
WPI Acc No: 1998-373436/199832
XRPX Acc No: N98-293081
High density mounting substrate for **mounting** SAW element **chip** - **mounts** SAW element **chip** on recess formed in **first** substrate **layer** by high viscosity epoxy resin
Patent Assignee: KOKUSAI DENKI KK (KOKZ)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10150273	A	19980602	JP 96309626	A	19961120	199832	B

Priority Applications (No Type Date): JP 96309626 A 19961120
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10150273	A		6	H05K-003/46	

Abstract (Basic): JP 10150273 A

The substrate has wiring patterns (6,24) formed on a multilayered PCB (20) which bonds a pair of substrate layers (21,22). Both the wiring patterns are mutually connected by a through-hole (25). A punching member of predetermined size is provided in the **first** substrate **layer**. A recess is formed in the punching member and in under surface of **first** substrate **layer**. A **first connection** pad (26) is arranged on both left and right sides in the recess.

A second connection pad (31) is connected to the first connection pad with a solder bump (32). A saw element chip (12) having a predetermined metal electrode pattern on its surface is formed on the recess. The chip is sealed by a high viscosity epoxy resin (33) whose viscosity is controlled during packing, such that it does not enter into **gap** formed between **first** substrate **layer** and **chip**.

ADVANTAGE - Reduces size and cost.

Dwg.1/4

66/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011393671
WPI Acc No: 1997-371578/199734
XRPX Acc No: N97-308608
Patient air mattress replacement system - comprises hose assembly containing number of supply tubes for providing air to air support layers, with valve fitting for preventing escape of air from support layers
Patent Assignee: HILL-ROM INC (HILL-N)
Inventor: ASHCRAFT D N; BRENNER J A; CHAMBERS K W; ELLIS C D; GLOVER S E; HAKAMIUN R; SALVATINI B
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5647079	A	19970715	US 96618757	A	19960320	199734	B

Priority Applications (No Type Date): US 96618757 A 19960320
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5647079	A		22		

Abstract (Basic): US 5647079 A

The system for use with a support bed frame comprises an air source and an air mattress replacement assembly for **mounting** on the bed **frame** and having a **first** air support **layer** and a **second** air support **layer**. A controller assembly is connected to the air source for selectively directing air to the **first** support **layer** and the **second** support **layer**. A

hose assembly system is provided for connection to the air source for communicating air from the air source to the mattress assembly. The hose assembly having a **first layer** supply tube for providing air to the **first layer** and a **second layer** supply tube for providing air to the **second layer**.

An interface connection assembly connects the mattress assembly to the hose assembly. The connection assembly communicates air from the **first layer** support tube to the **first** support **layer** and air from the **second layer** support tube to the **second** support **layer**. The **connection** assembly has a first valve fitting for preventing escape of air through the interface connection assembly from the **first** air support **layer** when the hose assembly is **disconnected** from the interface connection assembly.

USE/ADVANTAGE - For hospitals and clinics. Provides comfort and/or therapeutic support to bedridden patient.

Dwg.1,2/15

66/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010680784
WPI Acc No: 1996-177739/199618
XRAM Acc No: C96-056036
XRPX Acc No: N96-149425
Soldering semiconductor flip chip to circuit substrate - comprises attaching solder bump, and encapsulating in two resins, first having larger Young's modulus than other
Patent Assignee: TOSHIBA KK (TOKE)
Inventor: DOI K; HIRANO N; HIRUTA Y; MIURA M; OKADA T
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8055938	A	19960227	JP 94211711	A	19940815	199618	B
US 5629566	A	19970513	US 95512165	A	19950807	199725	

Priority Applications (No Type Date): JP 94211711 A 19940815
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8055938	A		8	H01L-023/28	
US 5629566	A		12	H01L-023/12	

Abstract (Basic): JP 8055938 A
The connection process involves attaching a semiconductor element (1) to a circuit substrate (2) by a solder bump (3). The solder bump is connected to the circuit substrate by a wiring **layer** (8). A **first** resin (41) is filled up in the central part and a second resin (42) is filled up in the peripheral part of the **gap** between the semiconductor element and the circuit substrate. The Young's modulus of the first resin is larger than that of the second resin. The first resin is harder than the second resin and has a filler.
ADVANTAGE - Enables reliable fixing of semiconductor element. Improves reliability over long period of time. Facilitates casting between circuit substrate and semiconductor element. Improves connection operativity.
Dwg.2/13
Abstract (Equivalent): US 5629566 A
A semiconductor device comprising: at least **one** semiconductor **chip mounted** on a circuit substrate and electrically **connected** to a metallization **layer** of the circuit substrate, a row of solder bumps being between a peripheral portion of the semiconductor chip and the metallization layer of the circuit substrate; a first encapsulant filling a first space between the semiconductor chip and the circuit substrate in the central portion of the semiconductor **chip**; and a **second** encapsulant filling a second space, exclusive of the first space, between the semiconductor chip and the circuit substrate in the peripheral portion of the semiconductor **chip**, the **second** space including the row of solder bumps totally within it, where the first encapsulant has a larger Young's modulus than the second encapsulant.
Dwg.10/14

66/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010395934
WPI Acc No: 1995-297247/199539
XRPX Acc No: N95-225488

Multi-chip module mfg. method - involves forming cementing layer between support substrate and mounting substrate initially and separating them after arranging wiring layers

Patent Assignee: FUJITSU LTD (FUIT)
Inventor: KURAMOCHI T

Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7193184	A	19950728	JP 93333354	A	19931227	199539	B
US 5521122	A	19960528	US 94297559	A	19940831	199627	
US 5654590	A	19970805	US 94297559	A	19940831	199737	
			US 96593337	A	19960129		

Priority Applications (No Type Date): JP 93333354 A 19931227
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7193184	A		11		
US 5521122	A		17		
US 5654590	A		17		Div ex application US 94297559 Div ex patent US 5521122

Abstract (Basic): JP 7193184 A

The **multi-chip module** mfg. method involves forming a cementing layer (11) on a support substrate (10). Multiple wiring layers (13,16,18) are stacked one above the other with insulated layers (12,15,17,19,21,23) in between, on a **chip mounting** substrate (26). The mounting substrate is formed above the cementing layer.

A hole (27) is formed which penetrates the insulating layers and mounting substrate and reaches the cementing layer with the use of an etching fluid (28) which is loaded through the hole to the cementing layer, the support substrate and the mounting substrate are separated.

ADVANTAGE - Prevents peeling off of interlayer insulating films and **disconnection** of wiring layer. Simplifies manufacturing process as hole is formed along with formation of mounting substrate.

Dwg.1/13

Abstract (Equivalent): US 5654590 A

A **multichip module**, comprising:

at least **one** semiconductor **chip**;

a **chip-mounting** substrate supporting the semiconductor **chip**, said **chip-mounting** substrate being constructed with at least **one** interlayer-insulating **layer** and at least **one** interconnection **layer**, at least **one** throughhole directing a treatment medium into a bonding **layer connecting** a supporting base and said **chip-mounting**

substrate in order to melt the bonding layer, and a flat and smooth under-surface formed on said **chip-mounting** substrate due to melting of the bonding layer; and

bumps interposed between said semiconductor **chip** and said **chip-mounting** substrate for fixing said semiconductor **chip** to said **chip-mounting** substrate and forming at least an electrical connection between said semiconductor chip and said interconnection layer of said **chip-mounting** substrate;

wherein the supporting base supports said **chip-mounting** substrate during information of said **chip mounting** substrate, and after said **chip-mounting** substrate is formed, the supporting base is removed from said **chip-mounting** substrate by leading the treatment medium into said throughhole and melting the bonding layer, and subsequent to removal of the supporting base, said semiconductor **chip** is **mounted** on said **chip-mounting** substrate through said bumps to form the **multichip module**.

Dwg.12/15

US 5521122 A

A **multichip-module** fabrication method comprising the steps of:

(a) forming a **chip-mounting** substrate by forming a bonding layer on a supporting base and by forming one or a plurality of interconnection layers in a stack formation on the bonding layer via insulating layers;

(b) forming one or a plurality of throughholes extending through said insulating layers to said bonding layer on said **chip-mounting** substrate;

(c) separating said supporting base from said **chip-mounting** substrate by leading a treatment medium which is capable of removing said bonding layer to said bonding layer at least through said one or plurality of throughholes; and

(d) **mounting** a semiconductor **chip** on said **chip-mounting** substrate.

9,10,11/15

66/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004008060
WPI Acc No: 1984-153602/198425
XRPX Acc No: N84-114087
Straddle-type grape and fruit orchard harvester - has end spacer releasably joined to hollow box-beam stringers fitted with plate for wheel legs
Patent Assignee: BRAUD SA (BRAU-N)
Inventor: DEUX A; MERANT J C
Number of Countries: 007 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 3343723	A	19840614	DE 3343723	A	19831202	198425	B
GB 2131264	A	19840620	GB 8332500	A	19831206	198425	
FR 2536949	A	19840608				198428	
AU 8321825	A	19840614				198431	
ZA 8308787	A	19840606				198440	
ES 8502311	A	19850401				198524	
GB 2131264	B	19860716				198629	
IT 1167290	B	19870513				198940	

Priority Applications (No Type Date): FR 8220370 A 19821206
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 3343723	A		36		

Abstract (Basic): GB 2131264 A
An all purpose straddling machine comprising a main chassis and appliances for the cultivation, treatment and harvesting of in-line planted fruit bushes selectively attached to the main chassis, at least one of the appliances having a dimension in height considerably greater than the height of the main chassis above the ground, said main chassis comprising two parallel and substantially horizontal side members and a first cross spacing member, which is connected to the side members at one of the front and rear ends thereof each side member being provided with two arms, respectively front and rear, which extend substantially vertically downwards from the side member and which support at their lower ends wheels for rolling over the ground, said machine further comprising a removable further cross spacing member, which is detachably connected to said side members at the other of the front and rear ends and which, when fixed to said side members, forms with the side members and the first cross spacing member a rigid carrier frame defining a central space adapted to receive a chosen appliance for supporting a chosen appliance, whereby when said removable cross spacing member is **disconnected** from the side members of the main chassis, the chosen appliance can be inserted in or removed from the said central space by relative horizontal movement of the main chassis and appliance.
DE 3343723 A

The grape and fruit orchard harvester comprises a mainframe (1) and releasably **mounted** implements (8). The **frame** has **two** stringers (2) and front and rear transverse spacers (3,4) forming the equipment surround framework, assisted by front and rear legs (5) and ground wheels (6). **One** of the **spacers** is releasably **connected** to the stringers these composed of rectangular hollow box beams working with the elbow tubes forming the spacers.

A horizontal plate (15) fixed under each stringer beam reaches into the frame and the end of each tube elbow mounts an angle piece (19) releasably fitted to the stringer such that one angle arm abuts the inner vertical side of the stringer and the second arm rests on the plate and is bolted to this, thus also securing the wheel leg. Each implement package has a rear spacer allocated which remains on the equipment when this is removed from the frame and completes this when mounted

Abstract (Equivalent): GB 2131264 B

An all purpose straddling machine comprising a main chassis and appliances for the cultivation, treatment and harvesting of in-line planted fruit bushes selectively attached to the main chassis, at least one of the appliances having a dimension in height considerably greater than the height of the main chassis above the ground, said main chassis comprising two parallel and substantially horizontal side members and a first cross spacing member, which is connected to the side members at one of the front and rear ends thereof each side member being provided with two arms, respectively front and rear, which extend substantially vertically downwards from the side member and which support at their lower ends wheels for rolling over the ground, said machine further comprising a removable further cross spacing member, which is detachably connected to said side members at the other of the front and rear ends and which, when fixed to said side members, forms with the side members and the first cross spacing member a rigid carrier frame defining a central space adapted to receive a chosen appliance for supporting a chosen appliance, whereby when said removable cross spacing member is **disconnected** from the side members of the main chassis, the chosen appliance can be inserted in or removed from the said central space by relative horizontal movement of the main chassis and appliance.

66/3,AB/7 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

03211507
CAPACITOR

PUB. NO.: 02-187007 [JP 2187007 A]
PUBLISHED: July 23, 1990 (19900723)
INVENTOR(s): AMANO TOSHINORI
APPLICANT(s): MURATA MFG CO LTD [000623] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-007076 [JP 897076]
FILED: January 13, 1989 (19890113)
JOURNAL: Section: E, Section No. 987, Vol. 14, No. 461, Pg. 163, October 05, 1990 (19901005)

ABSTRACT

PURPOSE: To sucure safety by cutting current application when an excess current flows by **connecting two** electrode **films** formed with an insulating film put therebetween through a current application interruption device.

CONSTITUTION: **First** and **second** electrode **films** 2 and 3 are formed on opposite sides of a dielectric substrate 1. An insulating film 7 is provided on the upper surface of the film 3, on which film 7 a third electrode **film** 8 is formed. **One** end of a **lead** terminal 5 is **mounted** on the film 8, and the other end of an interruption unit a is **connected** to the **film** 3. On the other, **one** end of a **lead** terminal 4 is **mounted** on the film 2. In such a construction, it functions as a capacitor as power is applied between the terminals 4 and 5. An excess current flows, the interruption unit 9 is subjected to **disconnection** and the films 3 and 8 are insulated by the film 7. Thus, the current application is cut off.

68/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013904594
WPI Acc No: 2001-388807/200141
XRAM Acc No: C01-118528
XRPX Acc No: N01-285887
Dry ice pelletizer includes mesh surrounding second end of extrusion cylinder
Patent Assignee: ALLEN R G (ALLE-I)
Inventor: ALLEN R G
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6240743	B1	20010605	US 99435671	A	19991108	200141	B

Priority Applications (No Type Date): US 99435671 A 19991108
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6240743	B1		11	F25J-001/00	

Abstract (Basic): US 6240743 B1
Abstract (Basic):

NOVELTY - A dry ice pelletizer includes a mesh surrounding a second end of an extrusion cylinder opposite a first end. The mesh allows 360 degrees venting of gas from the extrusion cylinder.

DETAILED DESCRIPTION - A dry ice pelletizer having an external power source comprises a **frame**, and at least **one** extrusion cylinder **mounted** on the **frame** and having at least one injection port (53). A piston (30) is provided for slidably moving inside the extrusion cylinder. A die (24) is located on a first end of the cylinder opposite the piston. A liquid carbon dioxide (CO2) line connects liquid CO2 source to the injection port. Hydraulic cylinders are **mounted** on the **frame** for reciprocating the piston inside the extrusion cylinder. A mesh (52) surrounds a second end of the extrusion cylinder opposite the first end, and allows 360 degrees venting of the CO2 gas from the extrusion cylinder. A controller reciprocally operates the hydraulic cylinder from the external power source to move the piston in the extrusion cylinder in a compression cycle. When the piston is near the second end, the liquid CO2 is injected into the extrusion cylinder through the injection port and flashes inside. When the piston moves to the first end, solid CO2 formed in the extrusion cylinder as a result of the flashing is compressed into a solid block of dry ice and forced outward towards the die. When the piston moves to the second end, gaseous CO2 escapes through the mesh and the cycle repeats. A support structure adjacent the mesh is provided for withstanding compressive forces of the extrusion cylinder.

An INDEPENDENT CLAIM is also included for a method of retrofitting a dry ice pelletizer that forms dry ice pellets comprising **disconnecting** extrusion cylinder from a hydraulic cylinder and a die, removing liquid CO2 lines from injection ports, replacing the

extrusion cylinder with a shorter extrusion cylinder and a circumferential mesh, reconnecting hydraulic cylinders and the die to the shorter extrusion cylinder and the mesh, and reattaching the liquid CO2 lines to the injection ports of the cylinder.

USE - For forming dry ice used in the processing and preservation of meats and other foods.

ADVANTAGE - The invention increases the dry ice production rate without requiring the dry ice producer to purchase new, expensive machinery.

DESCRIPTION OF DRAWING(S) - The figure shows a partial exploded perspective view of the extrusion cylinder portion of the dry ice pelletizer.

Die (24)
Piston (30)
Hood (42)
Mesh (52)
Injection port (53)
Flanges (56, 57)
Spacer tubes (59)
pp; 11 DwgNo 3/6

68/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010404655
WPI Acc No: 1995-305969/199540
XRPX Acc No: N95-232115
Logic cube device of packaging system for TAB frame - has **connection** element which **connects layers** of substrate for heat compression
Patent Assignee: NCR INT INC (NATC); AT & T GLOBAL INFORMATION SOLUTIONS INT (AMTT); HYUNDAI ELECTRONICS AMERICA (HYUN-N); SYMBIOS LOGIC INC (SYMB-N)
Inventor: CRAFTS H S
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7202117	A	19950804	JP 94286305	A	19941121	199540	B
US 5497027	A	19960305	US 93159898	A	19931130	199615	

Priority Applications (No Type Date): US 93159898 A 19931130
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7202117	A		9	H01L-025/00	
US 5497027	A		12	H01L-023/02	

Abstract (Basic): JP 7202117 A
The logic cube device (10) consists of a taiwanese board (12). A back (14) is mounted perpendicularly on both sides of board. Number of substrates (16) are provided as layers. An electrical element (18) connects the chips of the layers and the backs. Thus the flow of air which passes through the **gap** of **multi-chip modules** gets compressed.
ADVANTAGE - Reduces repair cost. Increases life time.
Dwg.1/9
Abstract (Equivalent): US 5497027 A
A logic cube, comprising:
(a) a base plate;
(b) at least two backplanes mechanically mounted to the base plate;

(c) a plurality of substrates mechanically mounted between the backplanes and electrically coupled thereto, each substrate having voltage and ground vias, wherein the power planes and ground planes are sandwiched by dielectric and selectively connected to the vias;
(d) at least **one** logic **chip mounted** on each of the substrates;
(e) at least **one** interconnect **chip mounted** on each of the substrates; and
(f) each substrate having a chip-to-chip interconnect pattern therein for electrically interconnecting the backplanes, the logic chips and the interconnect chips

68/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008923182
WPI Acc No: 1992-050451/199207
XRPX Acc No: N92-038592
Disk drive without magnetic head-to-disk capacitive coupling - has magnetic circuit of magnetic head connected to same potential as disk to eliminate coupling
Patent Assignee: HEWLETT-PACKARD CO (HEWP)
Inventor: DAVIDSON R J; GAILBREATH S H
Number of Countries: 004 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 470349	A	19920212	EP 91110278	A	19910621	199207	B
US 5142425	A	19920825	US 90564935	A	19900809	199237	
EP 470349	A3	19920506	EP 91110278	A	19910621	199330	
EP 470349	B1	19960228	EP 91110278	A	19910621	199613	
DE 69117384	E	19960404	DE 617384	A	19910621	199619	
			EP 91110278	A	19910621		

Priority Applications (No Type Date): US 90564935 A 19900809
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 470349	A				
Designated States (Regional): DE FR GB					
US 5142425	A		8	G11B-005/17	
EP 470349	B1	E	11	G11B-005/012	
Designated States (Regional): DE FR GB					
DE 69117384	E			G11B-005/012	Based on patent EP 470349

Abstract (Basic): EP 470349 A
The magnetic head (10) for a magnetic disk (7) has the magnetic circuit of its transducer attached to an electrical connection (28) which is attached to ground (104) or a fixed. The electrical connection is the centre bond pad which is **disconnected** from the coil bond pad and connected to the magnetic circuit (12). This prevents capacitive charging and arcing between the disk and the magnetic pole tips and also prevents noise due to variable capacitive coupling between the coil and the disk.
The centre bond pad and the disk are connected to the frame of the drive.
USE/ADVANTAGE - Reduces errors and damage from capacitive effects. (11pp Dwg.No.7/7
Abstract (Equivalent): EP 470349 B
The magnetic head (10) for a magnetic disk (7) has the magnetic circuit of its transducer attached to an electrical connection (28) which is attached to ground (104) or a fixed. The electrical connection is the centre bond pad which is **disconnected** from the coil bond pad and connected to the magnetic circuit (12). This prevents capacitive charging and arcing between the disk and the magnetic pole tips and also prevents noise due to variable capacitive coupling

between the coil and the disk.

The centre bond pad and the disk are connected to the frame of the drive.

USE/ADVANTAGE - Reduces errors and damage from capacitive effects. (11pp Dwg.No.7/7)

EP-470349 A magnetic disc memory drive apparatus having a **frame** (5), at least **one** rotatable memory disc (7) on said frame, a magnetic head actuator (6) movably **mounted** on said **frame** and electrically connected to said frame, a magnetic head (10) on said actuator disposed to scan a surface of said at least one rotatable memory disc during rotation, and a magnetic head amplifier circuit (40), said magnetic head comprising (a) a pair of spirally wound coils (18, 20) each having an inner end and an outer end, (b) a thin film magnetic circuit comprising upper (12) and lower (22) thin film poles of magnetic material having first (52, 58) and second (16, 26) opposite regions, said thin film poles (12, 11) being disposed about and electrically isolated from said coils (18, 20), and said second opposite end regions (16, 26) of said thin film poles (12, 22) being disposed in proximity to one another outside of said coils adjacent said surface of said at least one rotatable memory disc (7), (c) electrical insulating means (34) supporting said coils (18, 20), (d) circuits (90, 80) connecting said outer ends (42, 36) of said coils (18, 20) to said magnetic head amplifier circuit (40), (e) a metallic thin **film** circuit 28) **connected** to said thin **film** magnetic circuit (12, 22) at a magnetic circuit junction (56), and (f) means (30) including said frame (5) for providing an electrical connection between said metallic thin film circuit (28) and said at least one rotatable memory disc (7) to maintain said thin film magnetic circuit (12, 22) and said at least one rotatable memory disc (7) at ground potential, and characterised in that said pair of spirally wound coils (18, 20) are disposed in a coil position one above the other with the inner ends (46, 48) of said coils (18, 20) electrically connected together and the outer ends (42, 36) of said coils (18, 20) physically separated from one another, said electrical insulating means (34) support said coils (18, 20) in said coil position one above the other within said thin film magnetic circuit (12, 22), in electrical isolation from one another and from said thin film magnetic circuit (12, 22), and said first opposite end regions (52, 58) of said thin film poles (12, 22) are connected together and define said magnetic junction circuit (56) adjacent said inner ends (46, 48) of said coils (18, 20) within said coils.

(Dwg.1/6

Abstract (Equivalent): US 5142425 A

With the disk and the magnetic pole tips of the magnetic circuit at the same potential, capacitive charging and consequent current flow or arcing or discharge noise between the two are prevented. Noise from current due to the variable capacitive coupling of the coil to the disk during disk rotation is also eliminated.

The thin film magnetic transducer is fabricated be depositing successive layers of an electrical insulating material, a magnetic material, insulating material, electrical conducting material for a planar coil, insulating material and magnetic for a planar coil, insulating material and magnetic material, in the order named on a substrate. The planar coil comprises spiral turns and the magnetic

material layers are joined with each other within the spiral turns of the coil and encircle the coil, providing a magnetic **gap** between pole tips outside the of the coil. A thin film extension of the magnetic circuit is part of a circuit which connects the magnetic circuit to the frame of the disk drive as are the disks, which is usually ground potential.

ADVANTAGE - Prevents capacitive coupling between the transducer and the disk of a disk drive system.

Dwg.7/7

68/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007137290
WPI Acc No: 1987-137287/198720
XRAM Acc No: C87-057137
XRPX Acc No: N87-102894
Wafer-scale integrated circuit device and method - in which chips are placed on substrate and bound together by binder to-fill **gaps**
Patent Assignee: FUJITSU LTD (FUIT)
Inventor: FUKUSHIMA T
Number of Countries: 006 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 222144	A	19870520	EP 86113735	A	19861003	198720	B
JP 62081745	A	19870415	JP 85222593	A	19851005	198721	
US 4907062	A	19900306	US 88258112	A	19881214	199016	
KR 9008018	B	19901029				199207	
EP 222144	B	19920325	EP 86113735	A	19861003	199213	
DE 3684557	G	19920430				199219	

Priority Applications (No Type Date): JP 85222593 A 19851005
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 222144	A	E	12		
Designated States (Regional): DE FR GB					
EP 222144	B		15		
Designated States (Regional): DE FR GB					

Abstract (Basic): EP 222144 A
Semiconductor wafer-size IC device comprises: IC **chips** **mounted** on a substrate with their wired surfaces uppermost; binder of the same thermal expansion as the chips filling the inter-chip spaces, binding the chips to the substrate and to each other; an overall insulating layer except at the terminal pads; a wiring layer for interconnecting the chip terminal pads; and device pads to external circuitry. Pref. the binder is the same material as the chips, esp. poly- or amorphous-Si.
Pref. wiring layer is multi-layer structure. The **chips** are **mounted** in substrate depressions. The IC is mounted on a heat sink plate.
ADVANTAGE - A high performance **multi-chip** IC is provided at low cost.
7/10
Abstract (Equivalent): EP 222144 B
A -scale semiconductor integrated circuit device, comprising: (a) a plurality of integrated circuit chips (2); (b) a substrate (4) on which the **chips** are **mounted**, each with its wired surface upwards; (c) binder material (6), of essentially the same material as the material of the chips, having essentially the same thermal expansion coefficient as the thermal expansion coefficient of the chips, filling the **gaps** between the chips, whereby the chips are bound to the

substrate and to each other; (d) an electrically insulating layer (7) formed upon the wired surfaces of the chips and upon the binder material in the filled **gaps**, excluding portions where terminal pads of the chips are located; (e) electrically conductive layer-wiring (9) formed upon the insulating layer (7) for operatively interconnecting the chip terminal pads (8); and (f) one or more device terminal pads (10); for connecting the device to external circuitry, provided in connection with the electrically conductive layer-wiring (9). (15pp)a

Abstract (Equivalent): US 4907062 A

Interconnected multiple chips on which respective ICs are made are included in a semiconductor wafer-scale integrated device. Integrated circuit chips each have wiring and terminal pads. A passivation film is on the wiring. The chips are installed on a Si substrate and there is a binder in the **gaps** between the chips.

The binder, which is coplanar with the chips is made of monocrystalline-, polycrystalline-, or amorphous-Si. An insulating layer is on the wiring and the filled **gaps** except for the pads. A further wiring layer interconnects terminal pads and another terminal pad on the insulating **layer** is **connected** to an external circuit.

ADVANTAGE - High performance and low cost integrated circuit is obtd. (8pp)i

68/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004673981
WPI Acc No: 1986-177323/198628
XRPX Acc No: N86-132409
Flexible flat conductor for electronic circuits - has conductor pattern to accept surface **mounted chip** at **one** end
Patent Assignee: RAYTHEON CO (RAYT)
Inventor: CHERIFF F J; COX W N; KIRK J; PULVER A M
Number of Countries: 005 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 3545527	A	19860703	DE 3545527	A	19851220	198628	B
GB 2169750	A	19860716	GB 8530396	A	19851210	198629	
JP 61148706	A	19860707	JP 85287627	A	19851220	198633	
CA 1237817	A	19880607				198827	
GB 2169750	B	19890222				198908	
CA 1260623	A	19890926				198944	
US 5008656	A	19910416	US 90483345	A	19900220	199118	

Priority Applications (No Type Date): US 84684415 A 19841220; US 8797381 A 19870916; US 88173002 A 19880330; US 89325062 A 19890314; US 90483345 A 19900220
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 3545527	A		27		

Abstract (Basic): DE 3545527 A
The flexible connector for an integrated circuit chip comprises a flexible insulation substrate on which there are patterns of conductors. One conductor pattern also carries a number of solder points for connecting the chip. A cover layer with adhesive film protects the printed conductors and is placed between them and the chip. There are slots in the cover layer which correspond to the positions of the solder points.
The soler points project slightly through the cover layer and coiNcide with corresponding contact surfaces on the chip, which is of the surface mounting type. The connector section extends away from the chip as a flat conductor.
USE/ADVANTAGE - Driver circuit connection to flat screen indicator matrix. Allows very compact construction thus giving economy in use of space. (27pp Dwg.No.3/7)
Abstract (Equivalent): GB 2169750 B
A flexible cable assembly comprising a flexible insulating substrate having formed thereon a plurality of conductors; a prearranged group of solder pads disposed on the substrate, a plurality of said pads being electrically connected to said conductors; and circuit means having solder pads for attaching to said prearranged group of solder pads disposed on the substrate, wherein: a first portion of said plurality of conductors are disposed on a first side of the substrate and a second portion of said conductors are disposed on a

second side of the substrate, and said first portion of said plurality of conductors is covered by a top layer of the insulating substrate and said second portion of said plurality of conductors is covered by a bottom layer of the insulating substrate, the said top layer and said bottom **layer** being **attached** by adhesive means.t

Abstract (Equivalent): US 5008656 A

A display assembly has a display element for displaying a number of characters. A number of chip carrier device have driver circuits for selecting one or more of the characters. Flexible cables having insulated strip conductors, are readily connected and **disconnected** within the display assembly. A prearranged solder pad is disposed on a portion of a side of each one of the flexible cables for attaching **one** of the **chip** carrier devices.

Appts., disposed on a portion of a second side of each one of the flexible cables under the chip carrier device and attached to the flexible cables, has coefficient of expansion approximately matched to a coefficient of expansion of the chip carrier device. It restrains the flexible cables during temperature variations to accommodate the chip carrier device expansion. The disposed appts. provides support to each one of the flexible cables, further restraining them to prevent fatiguing at the solder pad.

ADVANTAGE - More readily repairable. (10pp

68/3,AB/6 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06808823
MULTICHIP MODULE CONNECTION STRUCTURE

PUB. NO.: 2001-036309 [JP 2001036309 A]
PUBLISHED: February 09, 2001 (20010209)
INVENTOR(s): ISHIKAWA MAKOTO
IZUMI ISAO
APPLICANT(s): NEC ENG LTD
APPL. NO.: 11-201835 [JP 99201835]
FILED: July 15, 1999 (19990715)

ABSTRACT

PROBLEM TO BE SOLVED: To stabilize a characteristic impedance at a connection part by providing a connection part of a dielectric substrate and a microwave(MM) IC chip with a **film**-shaped coplanar type **connection** line, in which a line is adhesion formed on a flexible film in parallel and mutually connecting signal lines of the dielectric substrate and the microwave IC chip.

SOLUTION: A microstrip line 3 on a dielectric substrate 2 is a structure, in which a **gap** is provided between a connection part grounding pattern 101 and itself, and the line forms a coplanar line with a grounding conductor. A **gap** between the connection part pattern 101 and the microstrip line 3, the width of the microstrip line 3 and their shape are set so that a transmission signal communicating through the microstrip line 3 is converted and transmitted efficiently to the coplanar line with the grounding conductor. The dielectric substrate 2 and an MMIC **chip** 6 **mounted** on it are mutually **connected** by a **film**-shaped coplanar type **connecting** line 100.

68/3,AB/7 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

04385455
LARGE-SCALE WIRING BOARD AND MANUFACTURE THEREOF

PUB. NO.: 06-029355 [JP 6029355 A]
PUBLISHED: February 04, 1994 (19940204)
INVENTOR(s): NARIZUKA YASUNORI
YAMAMURA HIDEO
TAKEDA KENJI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-180661 [JP 92180661]
FILED: July 08, 1992 (19920708)
JOURNAL: Section: E, Section No. 1544, Vol. 18, No. 238, Pg. 112, May 06, 1994 (19940506)

ABSTRACT

PURPOSE: To **mount** LSI **chips** on a multilayer wiring board at a high density with almost no **gaps** and obtain a compact large-scale wiring board capable of processing an electrical signal at a high speed.

CONSTITUTION: A plurality of LSI chips 1 are fixed on a smooth support board 2 with the chips adjoined without **gaps**, and an insulating layer 4 and a wiring layer 5 are formed on the surface of the LSI **chip** groups and a **first** board 30 is installed. A wiring board 40 on which a through hole 7a and a wiring pattern 8 are formed is mounted on the first board 30 and is bonded and fixed to the board 30. The inside of the through hole 7a is buried by a plating treatment, and a part between the lower wiring layer 5 and the upper wiring pattern 8 is electrically **connected** through a plating **layer** 9. By repeating the above mounting, bonding and fixing of the wiring board 40 and the electrical connection by the plating treatment, a multilayer board of the number of desired stacking layers is formed. By installing a cooling mechanism on the rear surface of the support board 2, the LSI chips 1 can be cooled effectively.

10/10/2002 09/818,440

10oct02 10:38:19 User267149 Session D375.1

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SYSTEM:OS  - DIALOG OneSearch
  File   2:INSPEC  1969-2002/Oct W1
         (c) 2002 Institution of Electrical Engineers
*File   2: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File   6:NTIS  1964-2002/Oct W1
         (c) 2002 NTIS, Intl Cpyrght All Rights Res
*File   6: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File   8:Ei Compendex(R)  1970-2002/Sep W5
         (c) 2002 Engineering Info. Inc.
*File   8: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File  34:SciSearch(R) Cited Ref Sci  1990-2002/Oct W2
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*File  34: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File 434:SciSearch(R) Cited Ref Sci  1974-1989/Dec
         (c) 1998 Inst for Sci Info
  File  35:Dissertation Abs Online  1861-2002/Sep
         (c) 2002 ProQuest Info&Learning
  File  65:Inside Conferences  1993-2002/Oct W1
         (c) 2002 BLDSC all rts. reserv.
  File  94:JICST-EPlus  1985-2002/Aug W1
         (c)2002 Japan Science and Tech Corp(JST)
  File  99:Wilson Appl. Sci & Tech Abs  1983-2002/Sep
         (c) 2002 The HW Wilson Co.
  File 144:Pascal  1973-2002/Oct W1
         (c) 2002 INIST/CNRS
  File 305:Analytical Abstracts  1980-2002/Sep W5
         (c) 2002 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate
removal, customized scheduling.  See HELP ALERT.
  File 315:ChemEng & Biotec Abs  1970-2002/Aug
         (c) 2002 DECHEMA
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10/10/2002 09/818,440

Set	Items	Description
S1	69	AU=(ANO, D? OR ANO K?)
S2	0	S1 AND (MULTICHIP OR MULTI()CHIP)
S3	2	S1 AND ((INTEGRAT??????(3N)(CIRCUIT?????? OR LOOP? ?)) OR - IC)
S4	67	S1 NOT S3
S5	0	S4 AND ((STACK?????? OR MOUNT??????)(3N)(CHIP? ? OR LEAD? ? OR FRAME? ?))
S6	0	S4 AND THERMOSET??????

10oct02 12:46:37 User267149 Session D377.1

SYSTEM:OS - DIALOG OneSearch
File 348:EUROPEAN PATENTS 1978-2002/Sep W05
(c) 2002 European Patent Office
File 349:PCT FULLTEXT 1983-2002/UB=20021003,UT=20020926
(c) 2002 WIPO/Univentio

STIC-EIC 2800 CP4-9C18 Irina Speckhard 308-6559

Set	Items	Description
S1	41477	((INTEGRAT??????(3N)(CIRCUIT?????? OR LOOP? ?)) OR IC)/TI,AB,CM
S2	14966	(CLOS??????(3N)(CIRCUIT?????? OR LOOP? ? OR PATH? ? OR ROUTE? ? OR ELECTRODE? ?))/TI,AB,CM
S3	55695	S1:S2
S4	396	((MULTICHIP? ? OR MULTI()CHIP? ?)(3N)(MODULE? ? OR ARRANGE??????))/TI,AB,CM
S5	528	((MULTICHIP? ? OR MULTI()CHIP? ?))/TI,AB,CM
S6	36438	((ONE OR FIRST OR TWO OR SECOND)(3N)(CHIP? ? OR LEAD? ? OR FRAME? ?))/TI,AB,CM
S7	36811	S4:S6
S8	36438	((ONE OR FIRST OR TWO OR SECOND)(3N)(CHIP? ? OR LEAD? ? OR FRAME? ?))/TI,AB,CM
S9	2051	((BOND?????? OR JOIN??????)(3N)(PAD? ? OR PADDING OR CUSHION?????))/TI,AB,CM
S10	38064	S8:S9
S11	16978	((STACK?????? OR MOUNT??????)(3N)(CHIP? ? OR LEAD? ? OR FRAME? ?))/TI,AB,CM
S12	2514	((BOND?????? OR JOIN??????)(3N)WIRE??????)/TI,AB,CM
S13	387	((BONDWIR??????? OR WIREBOND???? OR (WIRING OR WIRE????)(N)BOND???)(3N)(CHIP? ? OR LEAD? ? OR FRAME? ?))/TI,AB,CM
S14	2529	S12:S13
S15	94030	((ONE OR FIRST OR TWO OR SECOND)(3N)(LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR SPACER???))/TI,AB,CM
S16	14484	((ATTACH?????? OR CONNECT??????)(3N)(LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR SPACER???))/TI,AB,CM
S17	100135	S15:S16
S18	7596	THERMOSET??????/TI,AB,CM
S19	3	(THERMOSET??????(3N)(PLIAB?????? OR BENT OR BEND??????))/TI,AB,CM
S20	7596	S18:S19
S21	6284	((COUPL??????? OR LINK??????)(3N)(CHIP? ? OR LEAD? ? OR FRAME? ?))/TI,AB,CM
S22	1115	(ELECTRIC??????(3N)DISCONNECT??????)/TI,AB,CM
S23	58069	(DISCONNECT?????? OR GAP? ?)/TI,AB,CM
S24	58069	S22:S23
S25	3044	S3 AND S7
S26	2911	S25 AND S10
S27	560	S26 AND S11
S28	85	S27 AND S14
S29	32	S28 AND S17
S30	1	S29 AND S20
S31	31	S29 NOT S30
S32	0	S31 AND S20
S33	6	S31 AND S21
S34	6	IDPAT (sorted in duplicate/non-duplicate order)
S35	25	S31 NOT S34
S36	3	S35 AND S24
S37	3	IDPAT (sorted in duplicate/non-duplicate order)
S38	22	S35 NOT S36
S39	5	S38 AND S4
S40	5	IDPAT (sorted in duplicate/non-duplicate order)

S41	17	S38 NOT S39
S42	17	S41 AND S11
S43	17	S42 AND S8
S44	17	IDPAT (sorted in duplicate/non-duplicate order)

30/TI,PN,PD,PY,K/1 (Item 1 from file: 348)

IC card and method for manufacturing the same.
Karte mit **IC**-Baustein und Verfahren zur Herstellung derselben.
Carte a circuit integre et son procede de fabrication.
PATENT (CC, No, Kind, Date): EP 163534 A2 851204 (Basic)
EP 163534 A3 880824
EP 163534 B1 920923

IC card and method for manufacturing the same.
Karte mit **IC**-Baustein und Verfahren zur Herstellung derselben.

...ABSTRACT A2
IC card and method for manufacturing the same.
In an **IC** card according to the present invention, a base sheet (20) formed of thermoplastic material is sandwiched between a substrate sheet (24) and a dummy sheet (36) both formed of nonplastic material lower in thermoplasticity than the base sheet (20). The substrate sheet (20) is fitted with at least **one IC chip** (26) and input/output terminals (32) electrically connected to the **IC chip** (26). **First** and **second** cover sheets (40, 44) formed of thermoplastic material are put individually on the outer surface of the substrate sheet (24) and the dummy sheet (36...

...CLAIMS B1
1. An **IC** card comprising a base plate including at least **one IC chip** and input/output terminals electrically connected to the **IC** chip and cover means put on the base plate and having apertures through which the input/output terminals are exposed to the outside, said base...

...of thermoplastic material and having first and second surfaces; a substrate sheet adjacent the first surface of said base sheet and including said at least **one IC chip** (26) and said input/output terminals (32) electrically connected to the **IC** chip, said input/output terminals projecting from the other surface of said substrate sheet opposite to one surface thereof facing said base sheet; and a...

...formed of nonplastic material lower in thermoplasticity than said base sheet, which material is glass-reinforced epoxy resin, glass-reinforced triazine-based resin or other **thermosetting** resin, in that the further sheet is a dummy sheet (36) formed of glass-reinforced epoxy resin, glass-reinforced triazine-based resin or other **thermosetting** resin and similar in its mechanical strength and in its susceptibility to thermal contraction to the said substrate sheet (24), and in that the dummy sheet (36) and substrate sheet (24) have substantially the same shape and size.
2. The **IC** card according to claim 1, characterized in that the **IC chip** (26) is **mounted** on the one surface of said substrate sheet, and said substrate sheet includes first printed wiring means arranged on the one surface thereof so as to be

electrically connected to the **IC chip** by **wire bonding** and second printed wiring means arranged on the other surface so as to be electrically connected to the input/output terminals, the first and second printed wiring means being electrically connected via through holes (28) formed in said substrate sheet.

...cover sheet (40) formed of thermoplastic material to one surface of the intermediate plate on said substrate sheet side through a third sheetlike thermosensitive adhesive **film** (46), **attaching** a **second** cover (44) sheet formed of thermoplastic material to the other surface of the intermediate plate on said dummy sheet side through a fourth sheetlike thermosensitive adhesive film (46), and heating and pressing the intermediate plate and the first and second cover sheets for integration, each of the third thermosensitive adhesive **film** and said **first** cover sheet having apertures (42) as many as the input/output terminals through which the input/output terminals are passed.

11. The method according to claim 10, characterized in that in said first bonding process, the **IC chip** (26) is **mounted** on the one surface of the substrate sheet and embedded in a guard member (34) formed of **thermosetting** synthetic resin, and said base sheet is formed with an aperture (22) adapted to contain the **IC** chip embedded in the guard member when the base sheet and substrate sheet are joined together.
12. The method according to claim 11, characterized by...

34/TI,PN,PD,PY,K/2 (Item 2 from file: 349)

HIGH SPEED OPTICAL SUBASSEMBLY WITH CERAMIC CARRIER
SOUS-ENSEMBLE OPTIQUE A HAUTE VITESSE COMPRENANT UN SUPPORT CERAMIQUE
Patent and Priority Information (Country, Number, Date):
Patent: WO 200227874 A2 20020404 (WO 0227874)
Publication Year: 2002

Fulltext Availability:
Claims

English Abstract
...which extend into the terraced cavity along the trenches formed in the cavity. A vertical cavity surface emitting laser or vertically receiving optical element is **wire bonded** to the conductive traces which extend into the cavity. In one embodiment, the terraced cavity of the multilayer ceramic carrier includes a VCSEL and photodetector...

Claim
17 The multilayer ceramic carrier as in claim 9, further comprising an **integrated circuit** formed on said base surface and electrically coupled to said V(@SEL.
3 5
. The multilayer ceramic carrier as in claim 1, farther comprising a...

...ring and said corresponding pattern.
24 The multilayer ceramic carrier as in claim 1, further comprising a plurality of vias extending through at least a **first** ceramic **layer** of said ceramic **layers** and coupling a **first** 3 0 conductive trace formed above said **first** ceramic **layer** to a **second** conductive trace formed below said **first** ceramic **layer**.
3 5
. The multilayer ceramic carrier as in claim 1, ffirther comprising said optical source disposed on said base surface and capable of emitting light...

...ceramic carrier as in claim 27, ftirther comprising conductive leads extending from said bottom surface and capable of coupling said multilayer ceramic carrier to a **mounting** surface, said conductive **leads coupled** to said conductive traces formed on said bottom surface.
0

69 The optical component as in claim 68, wherein said **integrated circuit** comprises a laser diode driver. 0 70. The optical component as in claim 54, in which said cavity includes terraces forined on said interior sidewalls thereof, and at least one of said photodetector and said VCSEL are **wire bonded** to a conductive trace fon-ned on one of said terraces.
5

-4 0. The optical component as in claim 54, in which said cavity comprises a terraced cavity and said ceramic carrier comprises a multilayer ceramic carrier formed of a plurality of stacked ceramic **layers**, at least **two** of said ceramic **layers** including apertures therethrough, said apertures having a different size and wherein said respective apertures are aligned over one another to form said terraced cavity, at...top surface, said base section including a metallized bottom surface 0 being contenninouslyjoined to said top surface of said ceramic carrier, said metallized bottom surface **coated** with **one** of a polymer and a dielectric to enhance thennal expansion compatibility between said ceramic carrier and said optical housing.

34/TI,PN,PD,PY,K/4 (Item 4 from file: 349)

MULTIPLE CHIP MODULE WITH INTEGRATED RF CAPABILITIES
MODULE MULTIPUCE A FONCTIONS HF INTEGREES
Patent and Priority Information (Country, Number, Date):
Patent: WO 200045420 A2-A3 20000803 (WO 0045420)
Publication Year: 2000

Fulltext Availability:
Claims

English Abstract
...MCM) for use with baseband, RF, or IF applications includes a number of active circuit chips having a plurality of different functions. The active circuit **chips** are **mounted** on a substrate that is configured to provide an integrated subsystem in a single MCM package. The MCM includes a number of features that enable...

Claim
... at least one RF/1F active circuit chip configured to perform a plurality of RF/IF functions, said at least one RF/IF active circuit **chip** being **coupled** to said single interconnect substrate; and
at least one passive component coupled to said single interconnect substrate; wherein
said single interconnect substrate is configured to...

...integrate said plurality of RF/IF functions.

2 A multiple chip module according to claim 1, wherein said at least one RF/IF active circuit **chip** comprises a **first** RF/1F active circuit **chip** and a **second** RF/IF 1 5 active circuit chip having different electrical characteristics than said first RF/IF active circuit chip.

3 A multiple chip module according...

...and second RF/1F active circuit chips.
5 A multiple chip module according to claim 1 , wherein said at least one RF/IF active circuit **chip** comprises a **first** RF/IF active circuit chip configured in accordance with a first die technology and a second RF/IF active circuit chip configured in accordance with...

...array scheme, and a castellation array scheme.

8 A multiple chip module comprising:
a single interconnect substrate comprising an outer surface having a number of **wire bond** contact points resident thereon,
an RF/1F active circuit chip configured to perform at least one RF/1F function, said at least one RF/1F active circuit **chip** being

coupled to said number of
wire bond contact points with a like number of **wire**
bonds; and
a passive component surface-mounted to said single interconnect
substrate.

22 A multiple chip module according to claim 21, further comprising a die attach pad resident on an outer surface of said single...first and second RF/1F active circuit chips.

28 A multiple chip module comprising:
1 0 a single interconnect substrate;
an RF/1F active circuit **chip coupled** to said single
interconnect substrate, said first RF/1F active circuit **chip** having
a **first** portion configured to perform a first RF/1F function and a
second portion configured to perform a second RF/1F function;
wherein
1 5 said single interconnect substrate comprises a first ground plane
operatively associated with said first portion of said RF/1F active
circuit **chip** and a **second** ground plane operatively associated
with said second portion of said second RF/1F active circuit chip.

34/TI,PN,PD,PY,K/5 (Item 5 from file: 349)

CHIP STACK AND METHOD OF MAKING SAME
EMPILEMENT DE PUCES ET SON PROCEDE DE PRODUCTION
Patent and Priority Information (Country, Number, Date):
Patent: WO 9957765 A1 19991111
Publication Year: 1999

CHIP STACK AND METHOD OF MAKING SAME
Fulltext Availability:
Claims

English Abstract
A **stackable chip** carrier, made from plural layers of Kapton or other plastic material, and which may be made using conventional flex circuit techniques, has a central opening...

...apertures extending through the thickness thereof between opposite surfaces of the carrier and a conductive pattern therein which extends between the central opening and the **stacking** apertures. A **chip** is **mounted** within the central opening, and is electrically coupled to the conductive pattern such as by **wire bonding** or by soldering a ball grid array or other arrangement of contacts on the chip directly to the conductive pattern, and is encapsulated therein with potting compound using conventional chip-on-board encapsulation technology, to form a single layer **integrated circuit** element. Conductive elements such as metallic balls are inserted into the stacking apertures, and are mounted therein using solder or conductive epoxy, so as to electrically contact the conductive pattern and form a **stackable IC chip** package. A **stack** of the **chip** packages is assembled by arranging a stack of the packages so that the metallic balls which protrude from a surface of each package are inserted...

...an adjacent chip package, where they are electrically and mechanically secured by solder or conductive epoxy. Balls mounted within the stacking apertures of a lowermost **one** of the **chip** packages protrude from the bottom surface thereof, so that the completed **chip stack** forms a ball grid array product.

Claim
1 A **stackable chip** carrier comprising the combination of:
a base layer having a conductive pattern on at least one surface thereof,
a top layer mounted on the base...
...and
a plurality of stacking apertures extending through an entire thickness of the chip carrier defined by the base, top and center layers.

12 A **stackable chip** carrier in accordance with claim 7, wherein a portion of **one** of the **layers** of copper cladding extends between an adjacent pair of the stacking apertures, and the base and center layers have apertures therethrough adjacent the portion of

one of the **layers** of copper cladding, whereby a tool can be inserted through the apertures in the base and center layers to sever the portion of **one** of the **layers** of copper cladding.

18 A **stackable IC chip** package in accordance with claim 13, wherein the chip has a plurality of contacts thereon at opposite ends thereof, the chip carrier has a layer...

...contacts at opposite ends of the chip and a conductive pattern thereon having pads adjacent the openings in the opposite ends of the layer, the **pads** being **wire bonded** to the contacts at the opposite ends of the **chip**, the **stacking** apertures being spaced along opposite sides of the chip carrier between the openings in the opposite ends of the laver and the conductive pattern on the layer extending to the stacking apertures.

34/TI,PN,PD,PY,K/6 (Item 6 from file: 349)

IC CHIP PACKAGE AND METHOD OF MAKING SAME
BOITIER DE PUCE DE CIRCUIT INTEGRE ET PROCEDE DE FABRICATION DUDIT BOITIER
Patent and Priority Information (Country, Number, Date):
Patent: WO 9319485 A1 19930930
Publication Year: 1993

English Abstract
An **IC** chip package (12) and method of making the package (12) includes a chip having an upper active surface (34) bonded to the lower surface (42) of a substrate (24). Terminals (36) on the active surface (34) are **wire bonded** (32) through apertures (38) in a lower layer (24) of the substrate (22) to **bonding pads** (56) on the upper surface (46) of the substrate (24). Metallized strips (54) couple the **bonding pads** (56) to conductive pads (48) at the outer edges (50, 52) of the substrate (24). The substrate (22) includes an upper layer (26) having apertures (58) therein. After **wire bonding** (32), the apertures (58, 38) in the upper (26) and lower substrate layers are filled with epoxy (74), then the chip package (12) is electrically tested at various temperatures. The chip package (12) is programmed by **wire bonding** (32) a **chip** enable trace (37) to one of a plurality of optional **bonding pads** (57) of a **bonding** option array (55) on the lower substrate layer (24). The chip package (12) may then be assembled together with other chip packages (12) into a...

Claim
... chip package comprising the steps of:
providing a chip having a plurality of terminals on a surface thereof;
providing a substrate having a plurality of **bonding pads** on a surface thereof and at least one aperture therein;
attaching the chip to the substrate; and
wire bonding the terminals of the chip to the **bonding pads** of the substrate through the at least one aperture in the substrate,

2 A method of making a chip package in accordance with claim 1, comprising the further steps of:
filling the at least one aperture in the substrate with epoxy after the step of **wire bonding** the terminals is completed; and
grinding the epoxy flush with an upper surface of the substrate.
3 A method of making a chip package in...

...step of:
programming the chip package after the step of electrically testing the chip package is completed, the

34/TI,PN,PD,PY,K/3 (Item 3 from file: 349)

SURFACE MOUNT **IC** STACKING METHOD AND DEVICE
PROCEDE ET DISPOSITIF DE SUPERPOSITION DE CIRCUITS INTEGRES A MONTAGE EN SURFACE
Patent and Priority Information (Country, Number, Date):
Patent: WO 200068996 A1 20001116 (WO 0068996)
Publication Year: 2000

SURFACE MOUNT **IC** STACKING METHOD AND DEVICE
Fulltext Availability:
Claims

English Abstract
Packaged surface **mount** (SMT) **chips** having matched top contacts and bottom contacts are **stacked. Chip** features are selected to provide the desired **connectivity** between chip **layers** with a greater ease of manufacture. In one embodiment, additional spacing and routing layers are optionally provided between layers. In another, chips are differentiated by...

...substrate's contacts are configured for aligning with a dielectric region of a spacing layer or substrate to create very low capacitance signal paths between **stacked chips**.

Claim
1 A method of **stacking chips** by positioning at least **two chip layers** into an assembly fixture comprising a floor, each **layer** comprising at least **one chip**, the method comprising steps of:
(a) positioning a **first chip layer** directly on the floor;
(b) positioning a **first spacer layer** on the **first chip layer;**
(c) positioning at least **one** additional **chip layer** over the spacer layer;
(d) coupling the layers together; and
(e) removing the coupled layers from the assembly fixture, the coupled lavers comprising at least...

...nominal locations; in which each package has an interior, each interior and each die including several contacts; in which each of the conduits is a **bond wire** coupling one of the die contacts to one of the interior contacts;
in which installing steps (b) and (d) each comprise a step of coupling several **bond wires** each directlv to one of the die contacts and to one of the interior contacts; in which installing step (b) results in a first set...

...configuration.

5 A stacked device made by the method of claim 3.

6 A method of making a stacked device comprising at least a first **integrated circuit** (**IC**) die and a second **IC** die, comprising steps of:
(a) building a **first IC chip** having the **first** die in a first package;
(b) building a **second IC chip** having the **second** die in a second package, the second die being identical to the first die, the second package being internally identical to the first package;
(c) sealing the packages;
(d) modifying the electrical characteristics of at least **one** of the **chips**; and
(e) electrically coupling the **first chip** to the **second chip** to form a **stacked** device.
. The method of claim 6 in which the modifying step (d) comprises blowing at least one fusible link that resides on at least one of the dies.

9 A stacked device for coupling to a substrate comprising:
at least **two integrated circuit** (**IC**) **chips** comprising surface **mount** packages; and
stacking means for mechanically and electrically **coupling** the **IC** **chips** together.

10 A disc drive comprising the electrical system of claim 9, in which the stacking means is a set of solder contacts, in which...

...AMENDED CLAIMS
[received by the International Bureau on 30.March (30 00); original claim 3 amended; remaining claims unchanged (I page)]

1 A method of **stacking chips** by positioning at least **two chip layers** into an assembly fixture comprising a floor, each **layer** comprising at least **one chip**, the method comprising steps of:
(a) positioning a **first chip layer** directly on the floor;
(b) positioning a **first spacer layer** on the **first chip layer**;
(c) positioning at least **one** additional **chip layer** over the spacer layer;
(d) coupling the layers together; and
(e) removing the coupled layers from the assembly fixture, the

34/TI,PN,PD,PY,K/1 (Item 1 from file: 348)

Integrated **multichip** memory **module**, structure and fabrication.
Integrierter Multichipspeichermodul, Struktur und Herstellung.
Module de memoire integree **multichip**, structure et fabrication.
PATENT (CC, No, Kind, Date): EP 644547 A2 950322 (Basic)
EP 644547 A3 950712

Integrated **multichip** memory **module**, structure and fabrication.
Module de memoire integree **multichip**, structure et fabrication.

...ABSTRACT A2
An integrated **multichip** memory **module** structure and method of fabrication wherein **stacked** semiconductor memory **chips** are integrated by a controlling logic chip such that a more powerful memory architecture is defined with the appearance of a single, higher level memory...

...chips such that a single memory chip architecture with N M memory devices appears at the module's I/O pins. A preformed electrical interface **layer** is employed at **one** end of the memory subunit to electrically interconnect the controlling logic chip with the memory chips comprising the subunit. The controlling logic chip has smaller...
...layer and the controlling logic chip is secured to the electrical interface layer so as to reside within the lead frame, thereby producing a dense **multichip integrated circuit** package.
Corresponding fabrication techniques include an approach for facilitating metallization patterning on the side surface of the memory subunit. (see image in original document)

...CLAIMS A2
1. An integrated **multichip** memory **module** which emulates a single memory chip architecture, said integrated **multichip** memory **module** comprising:
a memory subunit having N memory chips wherein N >= 2, each memory chip of the memory subunit having M memory devices wherein M >= 2, along with two substantially parallel planar main surfaces and an edge surface, at least one planar main surface of each memory **chip** being **coupled** to a planar main surface of an adjacent memory chip of the memory subunit such that said memory subunit has a stack structure; and
logic...

14. A **multichip integrated circuit** package comprising:
a plurality of semiconductor **chips** of similar dimensions **coupled** together in a stack having an end surface and at least **one** side surface;
a **lead frame** secured to the **stack** at its end surface, said lead frame having an inner opening extending therethrough such that a portion of the stack's end surface remains exposed;
a semiconductor chip of smaller dimensions than the similar dimensions of the plurality of semiconductor **chips** forming the

stack, the semiconductor **chip** of smaller dimensions residing within the inner opening of the lead frame and being secured to the portion of the stack's end surface remaining exposed; and

metallurgy means for electrically interconnecting the plurality of semiconductor **chips** forming the **stack**, the semiconductor **chip** of smaller dimensions and the lead frame such that a dense **multichip integrated circuit** package is defined from semiconductor chips having different dimensions.

15. The **multichip integrated circuit** package of claim 14, wherein each semiconductor chip of said plurality of semiconductor **chips** comprises **one** of a logic **chip**, a memory chip, and a combination memory and logic chip.

16. The **multichip integrated circuit** package of claim 14, wherein said metallurgy means includes a plurality of transfer metallurgies electrically connected to said plurality of semiconductor chips, each transfer metallurgy being connected to **one** of said semiconductor **chips** of said plurality of semiconductor chips and extending to the at least one side surface of said stack, and wherein said metallurgy means further includes...

step of programming being carried out by **wire bonding** a **chip** enable trace to **one** of a plurality of optional **bonding pads** in a **bonding** option array located within the substrate,
Go A method of making a chip package in accordance with 1. wherein:
the chip has an active side...

...plurality
of terminals is located;
the substrate has a lower layer having a lower side and an opposite upper side on which the plurality of **bonding pads** is located; and
the step of attaching the chip comprises attaching the active surface of the chip to the lower side of the lower substrate layer.
7o A method of making a chip package in accordance with claim 6, wherein:
the step of **wire bonding** comprises coupling at least some of the plurality of terminals of the chip to corresponding ones of the plurality of **bonding pads** by **wires** extending through the at least one aperture in the substrate,
8o A method of making a chip package comprising the steps of:
providing a chip...

...an outer periphery defined by a plurality of outer edges;
the substrate has a plurality of electrical terminals therein; and
conducting the further step of **wire bonding** the plurality of electrical terminals of the chip to the plurality of electrical terminals of the substrate so that the **wire bonding** is confined ...chip package in accordance
with claim 10, comprising the further step of:
programming the coupling of one of the plurality of electrical terminals of the **chip** to **one** of the plurality of electrical terminals on the substrate after the step of electrically testing has been completed.

13 A method of making a **stack** of **chip** packages comprising the steps of:
making a plurality of chip packages, each having a chip attached to a substrate;
electrically testing each of the chip packages; and
assembling the electrically tested **chip** packages into a **stack**,

14 A **chip** package comprising the combination of:
a chip having opposite side edges defining a

37/TI,PN,PD,PY,K/1 (Item 1 from file: 348)

Connection for semiconductor devices or **integrated circuits** by coated wires and method of manufacturing the same.
Verdrahtung fur Halbleiterbauelemente oder integrierte Schaltungen durch beschichtete Drahte und Verfahren zu ihrer Herstellung.
Connexion pour dispositifs a semiconducteur ou circuits integres au moyen de fils gaines et procede pour sa fabrication.
PATENT (CC, No, Kind, Date): EP 355955 A2 900228 (Basic)
EP 355955 A3 911227

Connection for semiconductor devices or **integrated circuits** by coated wires and method of manufacturing the same.

...ABSTRACT A2
A semiconductor **integrated circuit** device (2) in which **wire bonding** is applied by using a **bonding wire** (5) having heat resistant polyurethane coating (5B), a semiconductor **integrated circuit** device applied with bonding by way of a coated wire and encapsulated with a resin composition (6) of a low heat expansion coefficient, and a semiconductor **integrated circuit** device free from **disconnection** and damage to the coated wire by applying chamfering to a chip, etc. ...

...CLAIMS A2
1. A method of manufacturing a semiconductor device in which external terminals of a semiconductor chip and a lead are **connected** by way of **coated** wires comprising a metal wire coated at the surface thereof with an insulative coating layer, wherein the coating layer for said coated wire comprises a
2. A method of manufacturing a semiconductor device as defined in claim 1, wherein the **coating layer** at **one** end of the **coated** wire is removed upon forming a metal ball, and said metal ball is connected to the external terminal of the semiconductor chip.

...the connection of said the other end to said lead.
6. A method of manufacturing a semiconductor device as defined in claim 1, wherein the **wire bonding** portion of the **lead** is particularly heated locally upon connecting the other end of the coated wire to said lead.
7. A method of manufacturing a semiconductor device as...

24. An intermediate layer forming apparatus as defined in claim 23, wherein baking means is disposed between said first storage reservoir and said second storage reservoir.
25. A semiconductor device in which external terminals of a semiconductor **chip mounted** on a tab and a lead are **connected** by way of **coated** wires each comprising a metal wire coated at the surface thereof with an insulator and said **coated** wire and the **connection** portion of said **coated** wire are covered with a resin, wherein the shape is

moderated at the corners for the semiconductor chip, corners for the tab and the corners...

...forming a semiconductor device by using a coated wire comprising a metal wire coated at the surface thereof with an insulator, which includes steps of **mounting** a semiconductor **chip** on a **first** package at a position of **mounting** said **chip**, connecting external terminals of said semiconductor chip and a lead by way of said coated wire to form a first semiconductor device, **mounting** a semiconductor **chip** identical with the semiconductor **chip** of said **first** semiconductor device on a second package of a kind different from that of the first package for said first semiconductor device at a position for **mounting** said **chip**, connecting the external terminals of said semiconductor chip and said lead by way of said coated wire to form a second semiconductor device.

37/TI,PN,PD,PY,K/2 (Item 2 from file: 349)

INTEGRATED VCO
OSCILLATEURS DE COMMANDE DE TENSION (VCO) INTEGRES
Patent and Priority Information (Country, Number, Date):
Patent: WO 200072446 A1 20001130 (WO 0072446)
Publication Year: 2000

Fulltext Availability:
Claims

Claim
... desired range of tuning frequencies to be produced by the VCO. The effects of component spread are magnified when a VCO is disposed on an **integrated circuit** substrate. Components constructed on an **integrated circuit** substrate typically have wide variations and component values. Thus, the variable capacitance devices used to tune voltage control oscillators are required to have a wider tuning range of capacitances to compensate for the spread in **integrated circuit** component values. Those having skill in the art would understand the desirability of having a voltage control oscillator capable of being **integrated** on an **integrated circuit** substrate that does not have the 3 5 problem of requiring a large variable capacitance tuning range. This type of device would necessarily provide higher **integrated circuit** yields by providing a VCO requiring less of a variable tuning voltage range, thus allowing a tunable VCO to be economically **integrated** onto an **integrated circuit**.
ACTIVE FILTER MULTI-TRACK INTEGRATED SPIRAL INDUCTOR FIGURES
FIG. 28a is a plan view of a multi-track spiral inductor suitable for **integration** onto an **integrated circuit**, such as one produced with a CMOS process; FIGS. 28b-28g illustrate various planar devices comprising inductor and transformer configurations suitable for incorporating multiple tracks... FIG. 65 is an illustration of an ESD device disposed between a connection to a **bonding pad** and power supply traces; FIG. 66 is an illustration of parasitic capacitance in a typical **bonding pad** arrangement on an **integrated circuit**; FIG. 67 is an illustration of a embodiment of a **bonding pad** arrangement tending to reduce parasitic capacitances; FIG. 68 illustrates a cross section of the **bonding pad** structure of FIG. 67; FIGS. 69a-69e illustrate various ESD protection schemes utilized in the state of the art to protect an **integrated circuit** from ESD discharge due to charge build up on a die pad; FIG. 70 illustrates an approach to pad protection during ESD event; FIG. 71...6 MHz band, and each carrier is allocated a certain bandw idth to transmit its signal. In FIG. I it is seen that there are **gaps** between channels 114, and also between carrier signals 1 1 6. It is necessary to leave **gaps** of unused frequencies between the carriers

and between the channels to prevent interference between channels and between carriers within a given 3 0 channel. This...

...provided as an off-chip component. This particular configuration allows for considerable savings in component parts costs by partitioning more and more functionality into the **integrated circuit chip** . Remote (off **chip**) **mounting** of the crystal resonator requires that electrical contact between the crystal resonator and the associated oscillator circuit, be made with interconnecting leads of finite length. In **integrated circuit** technology, these interconnecting leads are typically implemented as circuit pads and conductive wires formed on a PC board substrate to which package leads are bonded...MHz. The choice of resonant frequency is solely a function of a circuit designer's preference and necessarily depends on the frequency plan of an **integrated circuit** in which the system of the invention is used to provide periodic timing signals. Turning now to FIG. 12, there is depicted a simplified schematic...

..current biasing the varactor diode. To set the varactors tuning range a fixed capacitance 4513 is typically used. The fixed capacitor typically gets the tuned **circuit close** to a desired frequency, and the varactor fine tunes the desired frequency. In an alternate embodiment a network of discreetly switched capacitors may be used...

...DC blocking capacitors may be utilized to prevent current flow from the control voltage line 4533. A varactor is typically constructed as a diode having **two lead**

.**bandwidth and degrades noise performance because of the low pass filtering affect. Also, with this arrangement a core circuit 5902 must be distanced from the bonding pad** 5904 to allow for the power supply traces 6002, 6004 to pass between the pad and core. This prevents minimization of the distance between **bonding pad** and circuit core. Parasitic capacitance between power supply conductors and traces connecting the core to the **bonding pad** are not the only problem encountered with this configuration. In the current state of the art the **bonding pads** tend to increase parasitic capacitance. FIG. 66 is an illustration of parasitic capacitance in a typical **bonding pad** arrangement on an **integrated c**

37/TI,PN,PD,PY,K/3 (Item 3 from file: 349)

HIGH DENSITY **MULTICHIP** PACKAGE
BOITIER MULTIPUCE A HAUTE DENSITE
Patent and Priority Information (Country, Number, Date):
Patent: WO 9107777 A1 19910530
Publication Year: 1991

English Abstract
A package (400) for multiple semiconductor **integrated circuit** chips (110A-110D, 211, 416A, 416B) uses an interconnect structure (114, 426) manufactured by semiconductor processing techniques to provide dense interconnections between chips and to...

...are aligned by the frame (124) to connect pads on the interconnect structure top to traces on a mother board to which the package is **mounted. Chip** bonding plates (216) allow chips to be removed from the package and replaced when found defective.

Claim
le A **multichip** package having an interior and an exterior and comprising:
a heatsink;
a plurality of semiconductor **integrated circuit** chips thermally connected to said heatsinki including at least a **first chip** and a **second chip**, said **chips**
each having a plurality of I/O pads;
a plurality of conductors accessible at said exterior of said package;
an interconnect structure including:
means for connecting selected ones of said I/O pads of said **first chip** to selected ones of said I/O pads of said **second chipj** and
means for connecting selected ones f said I/O pads of at least some of said chips to selected ones of said plurality of conductors extending exterior to said package.

5* A **multichip** package as in Claim 1 in which said interconnect structure comprises:
a plurality of interconnect pads;
a plurality of conductive lines, each of said conductive lines interconnecting at least two of said interconnect pads;
means for connecting some of said interconnect pads to said I/O pads of said **first chip;**
means for connecting some of said interconnect pads to said I/O pads of said **second ch**

8 A multichip package comprising:
a heatsink;
a plurality of spaced semiconductor **integrated circuit** chips thermally connected to said heatsink,

said chips each having a plurality of I/O pads;
a multilayer interconnect structure placed near
but spaced from...
28 The **multichip** package of Claim 26, in which
said means for electrically connecting are **wire bonds**.
29* The **multichip** package of Claim 26, in which
said means for electrically connecting comprises TAB
bonding tape.
30e The **multichip** package of Claim 26, wherein
said frame is rectangular and includes a series of
20 peripheral rectangular through-slots for passage of said
means for connecting said exterior interconnect pads to
select ones of said points exterior to said mother board,
31 The **multichip** package of Claim 8, in which
said means for electrically connecting are **wire bonds**.

57 A **multichip** package having an interior and an
exterior and comprising:
a heatsink;
a plurality of semiconductor **integrated circuit**
chips thermally connected to said heatsink, including
at least a **first chip** and a **second chip**, said
chips
each having a plurality of I/O pads;

40/TI,PN,PD,PY,K/1 (Item 1 from file: 348)

Three-dimensional **multi-chip module** having **stacked** semiconductor **chips** and process of fabrication thereof
Dreidimensionaler Mehrchipmodul mit gestapelten Halbleiterchips und Herstellungsverfahren
Module tridimensionnel a plusieurs puces comprenant des puces semi-conductrices empilees et procede de fabrication
PATENT (CC, No, Kind, Date): EP 736903 A2 961009 (Basic)
EP 736903 A3 990127

Three-dimensional **multi-chip module** having **stacked** semiconductor **chips** and process of fabrication thereof

...ABSTRACT A2
A plurality of semiconductor chips (21a-21d) are sequentially bonded to one another so as to form a **stacked** semiconductor **chip** structure (21), and the **stacked** semiconductor **chip** structure is accommodated in a cavity (22a) formed in an insulating carrier (22); while the semiconductor chips (21a-21d) are being sequentially stacked, a conductive pattern (22c) formed on the bottom surface of the insulating carrier is connected to electrodes (21h/21i) on each of the semiconductor **chips** through **bonding wires** (23), and the three-dimensional **multi-chip module** is only slightly higher than the **stacked** semiconductor **chip** structure. (see image in original document) ...

...CLAIMS A2
1. A three-dimensional **multi-chip module** comprising:

an insulating carrier (22; 25; 29) including a major surface, an outer surface and conductive means (22b/22c; 25a/25f; 29f/29g) exposed to said major surface and said outer surface,

characterized by further comprising:
a **stacked** semiconductor **chip** structure (21; 26; 30) supported by said insulating carrier (22; 25; 29), and including a plurality of semiconductor chips (21a to 21d) each having an **integrated circuit** and conductive pads (21h/21i) formed in a peripheral area thereof and electrically connected to said **integrated circuit** and at least **one** insulating adhesive compound **layer** (21e/21f/21g) inserted between a central area of one of said plurality of semiconductor chips and a central area of another of said plurality...

...27: 31) connected between said conductive pads of said plurality of semiconductor chips and said conductive means of said insulating carrier.
2. The three-dimensional **multi-chip module** as set forth in claim 1, further comprising an insulating resin layer covering said conductive pads, said conductive means and said conductive wires.
3. The three-dimensional **multi-chip module** as set

forth in claim 1, in which said major surface defines a cavity (22a; 25b; 29c) where said **stacked** semiconductor **chip** structure is accommodated, the depth of said cavity being equal to or greater than the height of said **stacked** semiconductor **chip** structure.

4. The three-dimensional **multi-chip module** as set forth in claim 3, further comprising an insulating resin layer (24; 28; 32) filling said cavity so as to hermetically seal said **stacked** semiconductor **chip** structure, said conductive means and said conductive wires therein.

5. The module as set forth in any of claims 1 to 4, in which a...

...claims 1 to 6, further comprising a heat sink (33) attached to one of said plurality of semiconductor chips at the lowest position in said **stacked** semiconductor **chip** structure.

8. A three-dimensional **multi-chip module** comprising an insulating carrier for accommodating semiconductor chips,

characterized in that
said insulating carrier includes a plurality of insulating carrier members (41a-41d; 47) laminated...

...an opening (41e; 47d), an outer surface and conductive means (41f/41g) exposed to said first inner surface and said outer surface,
said three-dimensional **multi-chip module** further comprising:
a plurality of semiconductor chips (42a-42d; 48) each accommodated in said opening, each of said plurality of semiconductor chips having conductive pads (42g) formed on a first surface portion (42e), an **integrated circuit** formed in said first surface portion (42e) and a second surface portion (42f) removed therefrom; and
a plurality of sets of conductive wires (43; 50...

...of each of said plurality of semiconductor chips and said conductive means of one of said plurality of insulating carrier members.

9. The three-dimensional **multi-chip module** as set forth in claim 8, in which said first inner surface defines a cavity to which said opening (41e) is exposed.

10. The three-dimensional **multi-chip module** as set forth in claim 9, further comprising pieces of resin (44a-44d) each filling said cavity so as to not only hermetically seal said conductive pads, said conductive pattern and the set of conductive wires therein but also fix one of said plurality of semiconductor **chips** to associated **one** of said plurality of insulating carrier members.

40/TI,PN,PD,PY,K/2 (Item 2 from file: 348)

Ball grid package with **integrated** passive **circuit** elements.
Kugelrastergehause mit integrierten passiven Schaltungselementen.
Boitier a reseau de billes avec des elements de circuit passifs integres.
PATENT (CC, No, Kind, Date): EP 675539 A2 951004 (Basic)
EP 675539 A3 970521

Ball grid package with **integrated** passive **circuit** elements.

...ABSTRACT ball grid array arrangement comprises a dielectric multilayer substrate, in a lower metallisation layer of which is disposed an array of solder balls. A passive **circuit** element is **integrated** into at least **one** of the metallisation **layers**. The arrangement may be either a discrete component consisting of a triplate transmission-line resonator or interdigitated filter integrated into an inner metallisation layer and defined by that layer in conjunction with adjacent layers, or it may take the form of an **IC** carrier or **multichip-module** carrier having such transmission structures situated within a central die-attach area of the substrate and having also a peripheral area containing bonding structures for the mounting of at least **one chip** or **chip** module. There will normally be at least two groups of such bonding structures, and a passive circuit element in the form of an inductor may...

...CLAIMS A2

1. A ball grid array arrangement (10) including a dielectric multilayer substrate (12) having an upper, a lower and at least **one** inner **layer** of metallisation (30, 32, 31), the lower metallisation layer (32) including an array of solder balls (22), characterised in that a passive circuit element (60, 70, 75, 81, 100) is integrated into at least **one** of the metallisation **layers**.
2. A ball grid array arrangement as claimed in Claim 1, characterised in that the passive circuit element is a triplate line resonator transmission-line structure 60 formed in the at least **one** inner metallisation **layer** (31) and defined by that layer in conjunction with adjacent metallisation layers (30, 32) and intervening dielectric layers (33, 34).

8. A ball grid array arrangement as claimed in any one of the preceding claims, characterised in that the substrate includes a central, die-attach area (13) for the mounting of at least **one chip** or **multichip module** (24) and a peripheral area containing bonding structures (20) for establishing electrical connections between at least some of the solder balls (22) and the at least **one chip** or **multichip module** (24).

...ball grid array arrangement as claimed in any one of Claims 8 to 14, characterised in that the bonding structures in the peripheral area are **wire-bond pads** (20) formed in the upper metallisation layer (30), the pads (20) being either signal pads or ground or power supply pads (V1-V4), the pads...

...the bonding structures (20) are disposed between the central ground plane (13) in the upper metallisation layer and the peripheral seal ring (14).

19. A **multichip module** assembly characterised by including a ball grid array arrangement (10) as claimed in any one of Claims 8 to 18 and a **multichip module** (24) mounted on the ball grid array **arrangement** (10)

40/TI,PN,PD,PY,K/3 (Item 3 from file: 349)

PACKAGING AND INTERCONNECT SYSTEM FOR **INTEGRATED CIRCUITS**
SYSTEME D'ENCAPSULATION ET D'INTERCONNEXION DE CIRCUITS INTEGRES
Patent and Priority Information (Country, Number, Date):
Patent: WO 9736325 A1 19971002
Publication Year: 1997

PACKAGING AND INTERCONNECT SYSTEM FOR **INTEGRATED CIRCUITS**
Fulltext Availability:
Claims

English Abstract
...interconnect circuit (16) is fabricated on a thin aluminum wafer (22). The thin film decal interconnect (16) employs AU metallurgy for bonding and comprises a **bond pad**/ground plane **layer**, topside pads, and **one** or more routing **layers**. The top routing layer also acts as the pad layer along the edge of the interconnect structure (16). The underside of the decal interconnect structure (16) is provided with metal pads for attachment to conventional aluminum or gold I/O pads on one surface of the **integrated circuit** die (12). A thermosonic bonding system is used to **bond** the die **pads** (66) to the pads. The aluminum wafer is selectively removed forming one or more cavities (18, 20) to hold one or more die (12, 14...

...which they are bonded and cavities (18, 20) are filled with a liquid encapsulant (26) and cured. A lead frame has inner bond leads electrically **bonded** to **bonding pads** (122) of the thin film multilayer interconnect circuit disposed about periphery thereof and a multilayer laminate board is mechanically bonded over the thin film multilayer interconnect circuit (16) and over the inner bond leads of the lead frame (120) and has a **first layer** (124) including conductive pads (130) extending outward from about an inner periphery thereof, and a **second layer** including apertures (136) aligned with outwardly extending portions of the conductive pads (130). ...

Claim
I A **multichip module** packaging structure comprising:
a thin film multilayer interconnect circuit disposed on a baseplate, said baseplate including at least **one chip mounting** cavity formed therein, said thin film multilayer interconnect circuit comprising a layer including a plurality of first **bonding pads** disposed on a **first** surface thereof, a **layer** including a plurality of second **bonding pads** disposed on a second surface thereof, and at least **one** routing **layer** including a plurality of routing conductors; at least one **integrated circuit** die having first and second surfaces and disposed entirely within said at least **one chip mounting** cavity on said first surface of said thin film multilayer 1 0 interconnect circuit, said at least one **integrated circuit** die including a plurality of 1/0 connection pads disposed on said first surface thereof in contact with said first surface of said

thin film multilayer interconnect circuit, said at least one **integrated circuit** die-laligned so as to mate said plurality of I/O connection pads with said plurality of first **bonding pads**, said 1/0 connection pads electrically connected to said first **bonding pads**. 1 5 2. The **multichip module** packaging structure of claim I wherein said VO connection pads are electrically connected to said first **bonding pads** by solder ball reflow.

40/TI,PN,PD,PY,K/4 (Item 4 from file: 349)

PACKAGING AND INTERCONNECT SYSTEM FOR **INTEGRATED CIRCUITS**
SYSTEME D'ENCAPSULATION ET D'INTERCONNEXION DE CIRCUITS INTEGRES
Patent and Priority Information (Country, Number, Date):
Patent: WO 9427318 A1 19941124
Publication Year: 1994

PACKAGING AND INTERCONNECT SYSTEM FOR **INTEGRATED CIRCUITS**
Fulltext Availability:
Claims

English Abstract
...interconnect circuit (16) is fabricated on a thin aluminum wafer (24). The thin-film decal interconnect (16) employs Au metallurgy for bonding and comprises a **bond pad**/ground plane **layer**, topside pads, and **one** or more routing **layers**. The top routing layer also acts as the pad layer along the edge of the interconnect structure. The underside of the decal interconnect structure is provided with metal pads for attachment to conventional aluminum or gold I/O pads (60, 62, 64) on one surface of the **integrated circuit** die (12). A thermosonic bonding system is used to **bond** the die **pads** to the pads. The aluminum wafer is selectively removed forming one or more cavities (18) to hold one or more die (12) to be mounted...

...a liquid encapsulant (26) and cured. The composite structure may be lapped down to minimize overall package thickness and to expose the backsides of the **integrated circuit** die for thermal management.

Claim
1 A **multichip module** packaging structure comprising:
a thin film multilayer interconnect circuit disposed on a baseplate, said baseplate including at least **one chip mounting** cavity formed therein, said thin film multilayer interconnect circuit comprising a layer including a plurality of first **bonding pads** disposed on a first
0
surface thereof, a layer including a plurality of second **bonding pads** disposed on a second surface thereof, and at least **one** routing **layer** including a plurality of routing conductors; at least one **integrated circuit** die having first and second surfaces and disposed within said at least **one chip mounting** cavity on said first surface of said thin film multilayer interconnect circuit, said at least one **integrated circuit** die including a plurality of 1/0 connection pads disposed on said first surface thereof in contact with said first surface of said thin film multilayer interconnect circuit, said at least one **integrated circuit** die aligned so as to mate said plurality of I/O connection pads with said plurality of first **bonding pads**, said 1/0 connection **pads** thermosonically **bonded** to said first **bonding pads**.

2 The **multichip module** packaging structure of claim I further including a layer of encapsulant disposed over said at least one **integrated circuit** die in said at least **one chip mounting** cavity.

3 A **multichip module** packaging structure comprising:
20
SUBSTITUT. F. SHEEF (RULE 26)
a thin film multilayer interconnect circuit disposed on a baseplate, said baseplate including at least **one chip mounting** cavity formed therein, said thin film multilayer interconnect circuit comprising a layer including a plurality of first **bonding pads** disposed on a **first** surface thereof a **layer** including a plurality of second **bonding pads** disposed on a second surface thereof, and at least **one** routing **layer** including a plurality of routing conductors; at least one **integrated circuit** die disposed within said at least **one chip mounting** cavity on said first surface of said thin film multilayer interconnect circuit, said at least one **integrated circuit** die having a first surface bonded to said first surface of said thin film multilayer interconnect circuit in a position such that said plurality of first **bonding pads** of said thin film multilayer interconnect circuit are disposed about the periphery of said at least one **integrated circuit** die, said at least one **integrated circuit** die including a plurality of 1/0 connection pads disposed on a second surface thereof opposed to said first surface thereof, ones of said plurality of I/O connection **pads wire bonded** to corresponding ones of said plurality of first **bonding pads** of said thin film multilayer interconnect circuit.

40/TI,PN,PD,PY,K/5 (Item 5 from file: 349)

ARRANGEMENT FOR ENCASING A FUNCTIONAL DEVICE, AND A PROCESS FOR THE PRODUCTION OF SAME
CONFIGURATION POUR LA MISE EN BOITIER D'UN DISPOSITIF FONCTIONNEL, ET PROCEDE POUR SA FABRICATION

Patent and Priority Information (Country, Number, Date):
Patent: WO 9220096 A1 19921112
Publication Year: 1992

Fulltext Availability:
Claims

English Abstract
...functional device, e.g., a semiconductor element, a semiconductor-based element, a sensor element, a microactuator, or an electronic circuit consisting of one or more **integrated circuits** and other electronic components, and a process for preparing an arrangement of this kind. Around the functional device (47) is arranged a casing (43, 45...

...is made of a plastic material or another polymer material. The casing consists of two or more joined components (43, 45). Metal parts which form **wire bonds** (46) with said functional device (47) in the casing pass through the walls of said casing. At least one of the casing pass through the...

Claim
... between the diaphragms, The invention is also especially suitable for power components, ie, special high power semiconductors. The invention is also most suitable for encasing **integrated circuits**. Further, the invention can, with advantage be used on **multi-chip modules** which must be liquid cooled, comprising circuits of large area (up to the size of a circuit board) , and optionally also in several layers, In...
.60 may be a coupling board with an electronic function, comprising active devices, functional devices 57, 58 and 59, for instance in the form of **integrated circuits**, and connecting systems (not visible on the drawing), The base or board can comprise a **multilayer connecting** system, and can, as mentioned, be an integral part of the second casing component

62 For the electrical connections 65, 66, 67, 68, 69, and 70, and for the sake of simplicity, no **wire bonds** with said base 60 are shown. However, it will be understood that such **wire bonds** will necessarily be present, As is explained above, the two casing components 61 and 62 are brought together and thus a juncti on 75 is...

...6 is denoted by the

...respective wire members 187 and 188,
In the solution shown here, there is also the possibility of joining the two cavities together by means of **wire bond** 191 and
further to said functional device by means of wire members 192 and 193, respectively, The j oining of the top and base components...175; 189,190), eg, a semiconductor element, a semiconductor-based element, a sensor element, a microactuator, or an electronic circuit consisting of one or more **integrated circuits** and other electronic components, wherein the casing forms at least one closed cavity

44/TI,PN,PD,PY,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Semiconductor device having power distribution lines thereon
Halbleiterbauelement mit Leitungen zur Verteilung der Stromversorgung darauf
Dispositif semiconducteur ayant des conducteurs de distribution de puissance
PATENT (CC, No, Kind, Date): EP 1198004 A2 020417 (Basic)

...ABSTRACT A2
An **integrated circuit** (**IC**) **chip** (200), **mounted** on a leadframe, has a network of power distribution lines (251,252) deposited on the surface of the chip so that these lines are located over active components (202,203) of the **IC**, connected vertically by metal-filled vias (260) to selected active components below the lines, and also by conductors (240,241) to segments of the leadframe ...

...circuit level to the surface network. The network is electrically connected to selected active components by metal-filled vias. The network relocates most of the **bond pads** dedicated to power supply from the conventional alignment along the chip periphery onto the newly created bondable lines. The network is deposited and patterned in...
...electrical ground potential. The network has attachable outermost metal surface and is laid out so that network portions form pads convenient for attaching balls of **bonding wires** or solder.

...CLAIMS according to Claim 1 or Claim 2 further comprising:
said first and second plurality of active components (202a-202n;203a-203n) configured to form an **integrated circuit** comprising a plurality of active and passive electronic components arranged horizontally and vertically.
4. The device according to any preceding claim, wherein said active components (202a-202n;203a-203n) are configured in an **integrated circuit** that comprises a multi-**layer** metallization, at least **one** of said **layers** made of pure or alloyed copper, aluminum, nickel, or refractory metals.
5. The device according to any preceding claim, wherein said protective layer (230) comprises...

...and second conductors (251;252) are attached to outside parts by solder balls.
11. The device according to any preceding claim further comprising:
a metallurgical **attachment layer** that comprises **wire** ball and stitch **bonding**, ribbon bonding, and soldering.
12. The device according to any preceding claim, wherein said first and second conductors (251;252) comprise electrically conductive films that comprise at least **one** stress-absorbing metal **layer** selected from a group consisting of copper, nickel, aluminum, tungsten, titanium, molybdenum, chromium, and alloys thereof.
13. The device according to any preceding claim, wherein...

...of pure or alloyed gold, palladium, silver, platinum, and aluminum.

14. The device according to any preceding claim, wherein said third conductors (240;241) are **bonding wires, bonding** ribbons, or solder balls.

15. The device according to Claim 14, wherein said **bonding wire** is selected from a group consisting of pure or alloyed gold, copper, and aluminum.

16. The device according to Claim 14, wherein said solder ball...

...adapted to provide power distribution between said active circuit components.

19. A method for fabricating a semiconductor device including a semiconductor chip comprising:

forming an **integrated circuit** on a **first chip** surface, said circuit including active components, at least **one** metal **layer**, and a mechanically strong, electrically insulating protective overcoat;

forming a plurality of vias through said overcoat to access said at least **one** metal **layer**;

filling said vias by depositing a stack of metal films on said overcoat, said stack having at least **one** stress-absorbing **film** and an outermost film that is non-corrodible and metallurgically **attachable**;

patterning said **films** into a network of lines such that said lines are located substantially vertical over said active components and are suitable for power current distribution;

forming a plurality of windows in said overcoat to expose circuit contact pads;

providing a pre-fabricated leadframe comprising a **chip mount** pad, a **first** plurality of segments suitable for electrical signals, and a second plurality of segments suitable for electrical power and ground;

attaching said **chip** to said **chip mount** pad;

attaching electrical conductors to said circuit contact pads and said first plurality of segments; and

attaching electrical conductors to said network of lines and...

...according to Claim 19 wherein said steps of attaching electrical conductors to said contact pads and said network of lines comprise the step of either **bonding wires** or ribbons to said contact pads and network of lines, or reflowing solder balls to said contact pads and network of lines.

21. The method according to Claim 19 or Claim 20 further comprising the step of:

encapsulating said **chip, chip mount** pad, electrical conductors and at least a portion of said leadframe segments in a package.

44/TI,PN,PD,PY,K/2 (Item 2 from file: 348)

IC package and its assembly method
Integrierte Schaltungspackung und Verfahren zu ihrem Zusammenbau
Boitier pour circuit integre et methode d'assemblage
PATENT (CC, No, Kind, Date): EP 790653 A2 970820 (Basic)
EP 790653 A3 980415

IC package and its assembly method

CLAIMS 1. An **IC** package comprising:
a substrate having recesses formed on the side wall thereof;
an insulating film for covering an opening of each said recess on the side of a principal surface of said substrate; and
an **IC chip mounted** on a **mount** surface side of said film on said substrate, wherein a conductive portion formed on each said recess is used as an external connection terminal for said **IC** chip.

2. An **IC** package according to claim 1, wherein the whole principal surface of said **IC** chip on the **IC chip mount** side is sealed with insulating resin.

3. An **IC** package according to claim 1, wherein said insulating film covers only the opening and its peripheral area.

4. An **IC** package according to claim 1, wherein said substrate has a circuit pattern including a pad portion for electrical connection to said **IC chip**, an **IC chip mount** portion, and a wiring portion for connection of said pad portion and said **IC chip mount** portion to the conductive portion.

5. A method of assembling an **IC** package comprising the steps of:
forming a substrate having a plurality of through holes each having an insulating **film** covering **one** of the openings of each through hole;
mounting **one** or more **IC chips** on a principal surface of the substrate on the insulating **film** side, and electrically **connecting** the **IC** chip and the through holes;
sealing the substrate with the **IC chip mounted** thereon with insulating resin; and
cut the substrate with the **IC chip mounted** thereon to expose the side wall of each through hole.

6. A method according to claim 5, wherein said step of electrically connecting the **IC** chip to the through holes performs **wire bonding** between the **IC chip** and pad portions connected to the through holes.

44/TI,PN,PD,PY,K/3 (Item 3 from file: 348)

Multi-level **stacked** **integrated-circuit-chip** assembly
Mehrlagige, gestapelte **IC**-Anordnung
Assemblage de puces multicouches et empilees
PATENT (CC, No, Kind, Date): EP 782191 A2 970702 (Basic)

.ABSTRACT A2
A multi-level stack of **integrated circuit** has alternating chips and flip-**chips**, together with **wirebonds** that interconnect wiring pads (I/O pads) of the chips located on differing levels of the stack. In addition, solder bumps located between chips and ...

CLAIMS 1. A multi-level **stacked integrated-circuit-chip** assembly comprises:
(a) a first device comprising a wiring substrate or a **first integrated circuit chip**, a top major surface of the first device having at least a first wiring pad;
(b) second and third devices each comprising an **integrated circuit** chip or a wiring substrate, the third device located overlying the second device, the second device overlying the first device, a bottom major surface of the second device having **integrated circuitry** thereat and at least a third wiring pad; and,
(c) a wirebond directly electrically connecting the third wiring pad with the first wiring pad.
2...

...the top surface of the first device.
5. The assembly of claim 4 further comprising a fourth and fifth devices each of which comprises an **integrated circuit** chip or wiring substrate, the fifth device overlying the fourth device, the fourth device overlying the third device, the fourth device having at least a...
...on the top surface of the first device.
6. The assembly of claim 1 further comprising fourth and fifth devices each of which comprises an **integrated circuit** chip or a wiring substrate, the fifth device overlying the fourth device, the fourth device overlying the third device, the fourth device having at least...

44/TI,PN,PD,PY,K/4 (Item 4 from file: 348)

Semiconductor package stack module and method of producing the same
Stapelmodul von Halbleiterpackungen und Herstellungsverfahren
Module a empilement d'empaquetages de semi-conducteurs et procede de fabrication
PATENT (CC, No, Kind, Date): EP 729184 A2 960828 (Basic)
EP 729184 A3 991103

...ABSTRACT A2
In a semiconductor package stack module, an LSI (Large Scale **Integrated circuit**) is mounted, via fine bumps, on a ceramic carrier substrate or a flexible carrier film on which wiring conductors are formed. After a seal resin has been injected, the chip is thinned by, e.g., grinding. A plurality of such carrier substrates or carrier **films** are **connected** to each other by bumps via through holes which are electrically connected to the wiring conductors, thereby completing a tridimensional stack module. The module achieves a miniature, thin, dense, low cost, and reliable structure without resorting to a **wire bonding** system or a TAB (Tape Automated Bonding) system. In addition, the module has a minimum of wiring length and a desirable electric characteristic. (see image...

...CLAIMS through holes formed in said carrier or at end faces of said carrier;
a conductor pattern formed at least on a front of said carrier;
pads for inner **bonding**, and formed on a rear of said carrier, and electrically connected to said through holes; and
an LSI chip connected to said carrier by said...

...in said carrier and connected tridimensionally by electrically connected pumps for carrier connection.

3. A semiconductor package as claimed in claim 1, wherein said LSI **chip** is **mounted** on said carrier face down, and wherein said **pads** for inner **bonding** comprise bumps.
4. A semiconductor package as claimed in claim 3, wherein said **pads** for inner **bonding** and said bumps for carrier connection are formed of a solder whose major component is Pb-Sn, Sn-Ag, Sn-Zn, Au-Sn, Au, or...

...wherein said capacitor is electrically connected between a power source and ground.

12. A semiconductor package as claimed in claim 1, wherein said carrier comprises **one** of a **film**-like substrate of sintered ceramics, a flexible film, and a printed circuit board.
13. A semiconductor package as claimed in claim 12, further comprising an...

...each comprises through holes formed in or at end faces of said carrier, a conductor pattern formed at least on a front of said carrier, **pads** for inner **bonding**, and formed on a rear of said carrier, and electrically connected to said through holes, and an

LSI chip connected to said carrier by said...

...formed in said carrier and connected tridimensionally by electrically connected pumps for carrier connection.

18. A module as claimed in claim 16, wherein said LSI **chip** is **mounted** on said carrier face down, and wherein said **pads** for inner **bonding** comprise bumps.
19. A module as claimed in claim 18, wherein said **pads** for inner **bonding** and said bumps for carrier connection are formed of a solder whose major component is Pb-Sn, Sn-Ag, Sn-Zn, Au-Sn, Au, or In.
20. A module as claimed in claim 16, further comprising a heat radiator interposed between said LSI **chip mounted** on any **one** of said plurality of carriers and another carrier adjoining said one carrier, and closely contacting said carrier or said LSI chip.
21. A module as...

44/TI,PN,PD,PY,K/5 (Item 5 from file: 348)

A HIGH DENSITY **INTEGRATED CIRCUIT** ASSEMBLY COMBINING LEADFRAME LEADS WITH CONDUCTIVE TRACES
ZUSAMMENBAU EINER HOCHINTEGRIERTEN SCHALTUNG, DER LEITER EINES LEITERRAHMENS MIT LEITENDEN BAHNEN VERBINDET
CIRCUIT INTEGRE A HAUTE DENSITE COMBINANT DES CONDUCTEURS DE GRILLE DE CONNEXION ET DES RUBANS CONDUCTEURS
PATENT (CC, No, Kind, Date): EP 729645 A1 960904 (Basic)
EP 729645 B1 990317
WO 9608841 960321

A HIGH DENSITY **INTEGRATED CIRCUIT** ASSEMBLY COMBINING LEADFRAME LEADS WITH CONDUCTIVE TRACES

CLAIMS 1. An **integrated circuit** assembly comprising an **IC** chip (44) supported on the upper surface (34) of a dielectric substrate (32) that has defined thereon a predetermined array of electrically conductive traces (40, 52), a series of **bonding wires** (58A, 58B) respectively electrically connecting certain input/output pads 46B, 46D of the **IC** chip (44) to respective traces (40, 52), and further comprising a plurality of leadframe leads (48A-48D) bonded to the upper surface (34) of the dielectric substrate (32), characterised in that at least some of the leadframe **leads** 48B-48D are **stacked** on the upper surface (34) of the dielectric substrate (32) to overlie some of the traces (40, 52) and are electrically isolated from the traces (40, 52) by a layer (50) of insulating material, and a second series of **bonding wires** (56A-56D) respectively electrically connects other input/output pads (46A, 46C, 46E, 46F) of the **IC** chip (44) to respective leadframe leads (48A-48D).

2. An **integrated circuit** assembly according to claim 1 in which the lower surface of the substrate (38) has a plurality of solder balls (42) attached in predetermined positions...

10. An **integrated circuit** assembly (70) according to any preceding claim in which the **IC chip** includes at least **one** power terminal pad (84) and the circuit assembly further includes an electrically conductive layer (92) serving as a power plane supported by the substrate (72) stacked over at least some of the leadframe leads (80), means (81) for electrically isolating the conductive layer from the underlying leadframe **leads**, at least **one first bonding wire** (88) electrically **connecting** the conductive **layer** to the power terminal of the **IC chip**, and a **second bonding wire** (90) connecting the power plane to a preselected **one** of the leadframe **leads** or a preselected **one** of the conductive traces.

11. An **integrated circuit** assembly according to any of claims 1 to 9, said **IC** chip (82) includes at least one ground terminal and the circuit assembly further includes an electrically conductive layer (92) which serves as a ground plane...

...the substrate stacked over at least some of said leadframe leads (80), means (81) for electrically insulating the conductive layer (92) from the underlying leadframe **leads**, at least **one bonding wire** (88) electrically **connecting** the conductive **layer** to the ground terminal of the **IC chip**, and a **second bonding wire** (90) connecting the ground plane to a preselected **one** of the leadframe **leads** or a preselected **one** of the conductive traces.

44/TI,PN,PD,PY,K/6 (Item 6 from file: 348)

A direct chip attach module (DCAM).
Modul zur direkten Befestigung von Chips (DCAM).
Module d'attachement direct de puces (DCAM).
PATENT (CC, No, Kind, Date): EP 592022 A1 940413 (Basic)

...ABSTRACT A1
A low cost Surface Mount Carrier (SMC) for carrying **integrated circuit chips mounted** thereon. The carrier, or interposer, is a thin-small single layer or, a multi-layer deck of printed circuit board (FR-4) material with at least **one** direct **chip** attach (DCA) site for **mounting** a semiconductor **chip**. The DCA site has chip **bonding pads** wherein the **integrated circuit chip's pads** are **wire bonded** to or soldered to the carrier. The **bonding pads** are connected to wiring pads through interlevel vias and wiring lands or traces which may be on one of several wiring planes. The carrier is...

...CLAIMS A1
1. A carrier for carrying at least **one integrated circuit chip mounted** thereon, said carrier comprising: carrier connection means for providing power and signals to said carrier;
chip mounting means for fixedly mounting each of said at least **one integrated circuit chips** to said carrier; and
distribution means for distributing said power and said signals to said at least **one integrated circuit chip**, said distribution means comprised of a plurality of lands, and, at least **one layer** of a resin fiberglass composite material.

8. The carrier of any of claims 1-7 wherein the **chip mounting** means includes a plurality of chip **bonding pads** and a deposited solder ball on each of said plurality of chip **bonding pads**.
9. The carrier of any of claims 1-8 further comprising a lead frame, said **lead frame** being fixedly **mounted** by said carrier connection means.
10. The carrier of any of claims 1-9, further comprising a deposited encapsulant, whereby the **chip mounting** means for every **integrated circuit chip mounted** on said carrier is coated and protected by said deposited encapsulant.
11. An **integrated circuit** module comprising:
a carrier, said carrier comprising:
chip mounting means for fixedly mounting each of said at least **one integrated circuit chips** to said carrier, and
distribution means for distributing said power and said signals to said at least **one integrated circuit chip**, said distribution means comprised of a plurality of carrier pads connected to a plurality of chip **bonding pads** by carrier

wiring on at least one conductive plane, said conductive plane being on at least **one layer** of a resin fiberglass composite material;

16. The **integrated circuit** chip module of any of claims 11-15 wherein said **integrated circuit** chip package is a leaded chip carrier with a cavity and a plurality of package **wire bond pads**, and said **chip mounting** means comprises: a plurality of carrier **wire bond pads**; and a **wire bond** between each of said carrier **wire bond pads** and one of said package **wire bond pads**, whereby said carrier is fixedly mounted in said cavity.

44/TI,PN,PD,PY,K/7 (Item 7 from file: 348)

Package for microwave **IC**
Packung fur Mikrowellen-**IC**
Empaquetage pour circuit integre a micro-ondes
PATENT (CC, No, Kind, Date): EP 486273 A1 920520 (Basic)
EP 486273 B1 960911

..ABSTRACT A1

A microwave **IC** package comprises a base (1) and a plurality of cavities (2a) and (2b) for **mounting IC chips** (5a) and (5b), the cavities (2a) and (2b) being formed on the base (1). Also provided on the base (1) are terminals (4a), (4b), (8a), (8b) and (8c) which are connected to said **IC chips** by **wire bonding**. The cavities (2a) and (2b) are separated from each other by a grounded conductor (3A). Due to the separation, isolation between the input and the output of the **IC** package is improved. (see image in original document)

...CLAIMS A1

1. A microwave **IC** package, comprising:
   a base;
   a plurality of cavities provided on said base for **mounting IC chips**;
   at least **one** ground conductor provided on said base for partitioning off said cavities; and
   at least one terminal provided in said base and connected to said **IC** chips.

44/TI,PN,PD,PY,K/8 (Item 8 from file: 348)

Semiconductor memory device.
Halbleiter-Speicheranordnung.
Dispositif semi-conducteur de memoire.
PATENT (CC, No, Kind, Date): EP 398628 A2 901122 (Basic)
EP 398628 A3 910925

...ABSTRACT A2

A semiconductor memory device (1) comprising a supporting board (3), a plurality of semiconductor **IC** chips (4) arranged on the supporting board, in which interconnection is provided between the semiconductor chips and between the semiconductor chip and the supporting board. On the portion of the upper surface including the active area, of the semiconductor chip such as a memory **IC** chip bonding electrodes are arranged so as to extend substantially toward the confronting side. A plurality of such a memory **IC** chip are arranged on a single supporting board and the adjacent memory **IC** chips are directly connected by means of a **bonding wire** (6) or the like. Accordingly, this semiconductor memory device allows predetermined semiconductor **IC chips** to be **mounted** more densely and more compactly without requiring arrangement of conductive patterns (5) for connecting the semiconductor **IC** chips on a circuit board.

3. A semiconductor memory device as claimed in claim 2, wherein said semiconductor **IC** chip with said bonding electrodes arranged comprises a passivation film formed on a portion of the upper surface of said semiconductor **IC** chip excluding **bonding pads**, a **first** insulating **layer** formed on said passivation film, interconnection patterns formed on said insulating **layer** and **connected** to said **bonding pads**, a **second** insulating **layer** formed on said interconnection patterns excluding a portion of said interconnection patterns, and conductive patterns farmed on said **second** insulating **layer** and electrically **connected** to said interconnection patterns.

44/TI,PN,PD,PY,K/9 (Item 9 from file: 348)

Integrated circuit device having an improved package structure.
Integrierte Schaltungsanordnung mit einer verbesserten Packungsstruktur.
Dispositif a circuit integre comprenant une structure d'empaquetage.
PATENT (CC, No, Kind, Date): EP 346061 A2 891213 (Basic)
EP 346061 A3 910403

...ABSTRACT A2

An **integrated circuit** device includes a package (11, 41) having first and second surfaces and first and second internal connection lines (13b, 41b). A semiconductor **integrated circuit chip** (16) is **mounted** on the first surface of the package. A first group of external connection terminals (15) is provided on the first surface of the package, and is electrically connected to the semiconductor **integrated circuit chip** through the **first** internal connection lines (13b). A second group of external connection terminals (18) is provided on the second surface of the package so as to form a matrix arrangement of terminals, and is electrically connected to the semiconductor **integrated circuit chip** through the **second** internal connection lines (41b). The second group of external connection terminals includes specific terminals (18-2) specifically passing signals to be supplied to or from the semiconductor **integrated circuit** chip. The signals passing through the specific terminals are signals used at the time of evaluating the semiconductor **integrated circuit** chip.
...

...CLAIMS A3

1. An **integrated circuit** device comprising
a semiconductor **integrated circuit** chip (16);
a package (11, 41) having first and second surfaces and first and second internal connection lines (13b, 41b), said semiconductor **integrated circuit chip** being **mounted** on the first surface of said package; and
a first group of external connection terminals (15) provided on the first surface of said package, said first group of external connection terminals being electrically connected to said semiconductor **integrated circuit chip** through said **first** internal connection lines (13b), characterized by comprising
a second group of external connection terminals (18) provided on the second surface of said package so as to form a matrix arrangement of terminals, said second group of external connection terminals being electrically connected to said semiconductor **integrated circuit chip** through said **second** internal connection lines (41b) and including specific terminals (18-2) specifically passing signals to be supplied to or from said semiconductor **integrated circuit** chip, said signals passing through said specific terminals being signals used at the time of evaluating said semiconductor **integrated circuit**

chip.
chip mounting layer and providing said **second** surface of said package, said second group of external connection terminals (18) being provided on said metallized insulating **layer**, and

that said **first** internal connection lines (13b) are formed in said **chip mounting** layer (12) and said **wire bondig** layer (13, 13-1, 13-2), and said second internal connection lines (41b) are formed in said metallized insulating layer (41).

11. An **integrated circuit** device as claimed in claim 10, characterized in that said metallized insulating layer (41) comprises a plurality of stacked layers (41-1, 41-2, 41-3).

12. An **integrated circuit** device as claimed in claim 10 or 11, characterized in that said metallized insulating layer (41) is formed of an insulating material to which said second internal connection lines are provided.

44/TI,PN,PD,PY,K/10 (Item 10 from file: 348)

Semiconductor chip having external terminals connected to corresponding leads by wires.
Halbleiterchip mit Anschlussklemmen mittels Drahte verbunden mit korrespondierenden Leitern.
Puce semi-conductrice comprenant des bornes reliees aux conducteurs correspondants par des fils.
PATENT (CC, No, Kind, Date): EP 276940 A2 880803 (Basic)
EP 276940 A3 900530

...ABSTRACT A2
A resin-encapsulated **integrated circuit** has a semiconductor chip (2) whose **bonding pads** (2A) are connected to corresponding leads (3A) by wires (4). In order to achieve the correct interconnection of pads (2A) and leads (3A) some of...

...rather than having interconnected pads and leads adjacent each other, as is normal.
The use of insulated wires also permits one or more of the **bonding pads** to be central on the chip rather than at its periphery, and some of the pads may be connected to remote leads. ...

.outer lead continuous thereto,
said each inner lead lying within said mold member, with said each outer lead protruding from said mold member; and
(e) **bonding wires** which respectively connect the inner leads of said leads and said pads corresponding thereto, said wires being encapsulated in said resin mold member; wherein at least one of said wires is formed with an insulator film over a whole circumference of a substantially full length thereof, and it is **wire-bonded** so as to intersect at least one of the other wires with respect to an orthogonal projection on said principal surface of said chip.
6. A semiconductor **integrated circuit** device as defined in Claim 5, wherein each of the other wires is formed with an insulator film over a whole circumference of a substantially full length thereof.
7. A semiconductor **integrated circuit** device as defined in Claim 6, wherein each of the large number of wires is subjected to ball wedge bonding.
8. A semiconductor **integrated circuit** device as defined in Claim 7, wherein said mold member is formed by transfer molding.
9. A semiconductor **integrated circuit** device as defined in Claim 8, wherein said insulator film as a coating of said each wire is removed at and near a part of said wire to be connected to the corresponding lead or **pad**, during a **bonding** process.
10. A semiconductor **integrated circuit** device as defined in Claim 9, wherein said coating consists principally of an organic resin.
11. A semiconductor device comprising:

(a) a semiconductor **chip** which has **first** and second principal surfaces;

(b) internal logic circuits which occupy a considerable area on said first principal surface of said chip;

(c) **bonding pads** in a large number of at least 50 to 200, which are disposed along peripheral sides of said chip,

said large number of pads including a first set, each element of which has a first function, and a second set, each element of which has a **second** function;

(d) **leads** in the large number of at least 50 to 200, which are so disposed that first ends thereof lie near outer sides of said peripheral sides of said **chip**;

(c) **second bonding pads** in a large number of at least 10 ...in the large number of at least 10 to 200, which are so disposed that first ends thereof lie near said peripheral sides of said **chip**;

(e) **bonding wires** in the large number of at least 10 to 200, which respectively connect said **first** ends of said **leads** and the corresponding **second pads**;

(f) a **coating bonding wire** which **connects** any one of said **first** ends of said **leads** and the corresponding **first** pad; and

(g) a resin mold member which encapsulates said **chip**, said **first** ends of said **leads**, said **bonding wires**, and said coated **bonding wire**.

22. A resin-encapsulated semiconductor **integrated circuit** microcomputer device as defined in Claim 21, wherein said **wire** is **joined** to said output **pad** on said **first** CPU **chip** by ball bonding and is **joined** to said input **pad** on said **second** CPU **chip** by wedge bonding.

44/TI,PN,PD,PY,K/11 (Item 11 from file: 348)

Semiconductor device having an encapsulating package.
Halbleiteranordnung mit einer Verkapselungspackung.
Dispositif semi-conducteur comprenant un empaquetage d'encapsulation.
PATENT (CC, No, Kind, Date): EP 239315 A1 870930 (Basic)
EP 239315 B1 910619

...ABSTRACT A1

A heat-resistant plastic-packaged semiconductor device comprises an **IC** chip (13) having contacts on one side, an island (12) on which the **IC chip** (13) is **mounted** with its opposite surface facing one side of the island (12), a low-adhesion layer (17) which is formed on the other surface of the island (12), external **leads** (11), **bondig wires** (14) for connection to the contacts on the **IC** chip (13) and inner ends of the external leads (11), a package (15) of moulded resin for encapsulating the **IC** chip (13), the low-adhesion layer (17), the **bonding wires** (14) and inner parts of the external leads (11), the moulding being provided with a vent hole (18) which extends to the vicinity of the...

44/TI,PN,PD,PY,K/12 (Item 12 from file: 348)

Electronic circuit interconnection system.
Verbindungssystem fur elektronische Schaltung.
Systeme d'interconnexion pour circuit electronique.
PATENT (CC, No, Kind, Date): EP 210380 A1 870204 (Basic)

...ABSTRACT making substrate having a plurality of circuit paths for use as a circuit board in an electronic circuit interconnection system (10) which provides high density **mounting** of ceramic **chip**-carrier **integrated circuit** devices or other beam-lead, dual-in-line (DIP), tape-automated-bonded (TAB), flip-**chip**, or direct-**mounted** i.c. devices (14) with **wire-bonded** interconnects or the like on an economical, dimensionally-stable, interconnection substrate (12) which has high heat dissipating properties. The substrate has glass components which are...

...4), pin mounting holes (16.6) and other typical substrate features in the etched patterns in multimetal laminated metal plates of selected thickness which are **coated** on **one** or both sides with glass frit fused to the plates. Where substrates with more than **one layer** are desired, glass-coated plates are stacked with pin mounting holes and the like aligned and the glass coatings are fused together. Metal vias extend..

5. A method as set forth in claim 4 further characterized in that the **integrated circuit chip** is **mounted** on a ceramic **chip**-carrier and said metal conductors are bonded to the chip-carrier to extend between the terminals and the circuit paths on the substrate means.

6. A method as set forth in claim 4 further characterized in that the **integrated circuit chip** is **mounted** on a pliable tape and said metal conductors are bonded to the tape to extend between the terminals and the circuit paths on the substrate means.

7. A method as set forth in claim 4 further characterized in that the **integrated circuit chip** is **mounted** on a metal **lead** frame, said metal conductors comprise frame leads, and the frame leads are bonded to said circuit paths on the substrate means, and additional conductors are bonded to the chip terminals and to the frame leads for electrically connecting the **integrated circuit** of the chip to the frame leads.

8. A method as set forth in claim 4 further characterized in that the **integrated circuit** unit is a flip-chip unit having said terminals located on **one** side of the **chip**, and said metal conductors comprise solder connection, the solder connection being fixedly bonded to the chip terminals and to the circuit paths on the substrate means.

9. A method as set forth in claim 4 further characterized in that said **integrated circuit chip** is **mounted** directly on one portion of said metal layer means in heat-transfer relation thereto, and said metal conductors are bonded to the chip terminals and...

...as set forth in claim 10 further characterized in that an additional metal layer means is secured in spaced, stacked, electrically insulated relation to the **first**-named metal **layer** means by fusing of additional glass means between said metal layer means.

13. A method as set forth in claim 12 further characterized in that said **first**-named metal **layer** means has an opening of substantial size formed therein during said selective etching thereof, and said additional metal layer means has a platform portion thereof...

44/TI,PN,PD,PY,K/13 (Item 13 from file: 349)

DUAL-DIE **INTEGRATED CIRCUIT** PACKAGE
BOITIER DE CIRCUIT IMPRIME A DE DOUBLE
Patent and Priority Information (Country, Number, Date):
Patent: WO 200143193 A2-A3 20010614 (WO 0143193)
Publication Year: 2001

DUAL-DIE **INTEGRATED CIRCUIT** PACKAGE
Fulltext Availability:
Claims

English Abstract
A dual-die **integrated circuit** package (10) having **two integrated circuit chips** (14, 16) "flip chip" attached to each other and with **one** of the **chips** (14) being aligned at a specified angle in relation to the other chip (16) to allow access to **bonding pads** on the surface of each **chip** for wirebonding connection into the **chip** package. In a **first** embodiment, the **two chips** are rectangular in shape and are aligned at an angle of 90 degrees with respect to each other, thus allowing the end portions of the...
...at angles of less than 90 degrees, such that corner portions of each chip are accessible for connection into the chip package. The invention allows **two** identically constructed **chips** to be used for doubling or even greater multiplication of the functionality or memory of the **IC** package, while still using the same package footprint as for a single chip. Also, being able to use **two chips** that are identically constructed from a wafer fabrication standpoint provides the advantage of requiring only one **IC** design process.

Claim
1 A dual-die **integrated circuit** package comprising:
a flat die-attachment surface having a plurality of external electrical contacts for connecting the package to external circuits,
a **first IC chip** having a **first** surface and a second surface, and having a plurality of **bonding pads** on the first surface, the second surface being mounted on the die-attachment surface,
a **second IC chip** having a **first** surface and a second surface, and being mechanically and electrically connected by its second surface to the first surface of the **first IC chip**, wherein the **second IC chip** is aligned at a specified angle in skewed relation to the **first IC chip** in a covering relation, with **bonding pads** on the first surface of the **first IC chip** remaining uncovered and electrically connected to the external electrical contacts of the die-attachment surface, and
an encapsulant material enclosing the **first** and **second IC chip** and covering a portion of the die

44/TI,PN,PD,PY,K/14 (Item 14 from file: 349)

METHOD OF ENCAPSULATING A CRYSTAL OSCILLATOR
PROCEDE D'ENCAPSULATION D'UN OSCILLATEUR A QUARTZ
Patent and Priority Information (Country, Number, Date):
Patent: WO 9630974 A1 19961003
Publication Year: 1996

Fulltext Availability:
Claims

English Abstract
A method of encapsulating a crystal oscillator (100). First, a dielectric material is assembled or connected to the bottom side of a **lead frame** (102). **Second**, oscillator components including a piezoelectric element, capacitors and an **integrated circuit** are attached on the lead frame (104). Third, an epoxy dam is dispensed around the periphery of the oscillator component locations (106). Fourth, an encapsulant...

...encapsulate the oscillator components (108). Fifth, the epoxy dam and encapsulant are cured (110). Thereafter, the oscillator is singulated from the lead frame and the **leads** are formed for **mounting** (112). ...

Claim
Claims
A method of making a surface **mountable-lead frame** crystal oscillator, comprising:
assembling a lead frame with a dielectric layer, the lead frame includes a plurality of cells having top and bottom surfaces;
attaching oscillator components to the top of the lead **frame**;
dispensing a predetermined **first** viscous material to form a dam substantially around a periphery of each cell;
substantially filling the dam with a second viscous material;
curing the first and second viscous materials; and
singulating each cell to form a surface-**mountable lead frame** crystal oscillator.

44/TI,PN,PD,PY,K/15 (Item 15 from file: 349)
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PRE-FORMED CHIP CARRIER CAVITY PACKAGE
MODULE A CAVITE POUR SUPPORT DE PUCES PREFORME
Patent and Priority Information (Country, Number, Date):
Patent: WO 8910005 A1 19891019
Publication Year: 1989

Fulltext Availability:
Claims

English Abstract
A flexible circuit film (14) is used in a surface **mountable** pre-formed **chip** carrier cavity package as a direct interconnect between the **integrated circuit** chip (16) and external **bonding pads** on a printed circuit board. The **IC** chip carrier of the present invention is comprised of a square or rectangular base (12) having a central cavity (22); an **IC chip mounted** in the cavity and held therein by an adhesive (34); a lid (18) having a complementary shape to the upper surface of the base; and ...

...cuts or cutouts therein depending upon the specific package construction. Etched copper circuitry on the flex circuit forms interconnects between I/O pads on the **IC** chip and the outer periphery of the package (10). The package enables the use of more than 80 and up to more than 300 I...

...printed circuit board by solder connections between the exposed leads at the outer periphery of the package and conductive areas on the PC board surface. **Multi-chip** packages are also included.

Claim
le A surface **mountable integrated circuit chip** carrier
package comprising:
a first body portion, said first body portion having an upper and a lower surface;
a second body portion, said second body...

...said second body portion;
said first and second body portions being joined together so, as to define a chip cavity therebetween for receiving at least **one integrated circuit chip;**
at least **one integrated circuit chip** disposed within the
chip cavity;
a flexible circuit comprising a layer of flexible polymer **ic** film having a conductive circuit pattern thereon sandwiched between said upper surface of said first body portion and said

44/TI,PN,PD,PY,K/16 (Item 16 from file: 349)

PACKAGING SYSTEM FOR STACKING **INTEGRATED CIRCUITS**
SYSTEME DE CONDITIONNEMENT PERMETTANT D'EMPILER DES CIRCUIT INTEGRES
Patent and Priority Information (Country, Number, Date):
Patent: WO 8808203 A1 19881020
Publication Year: 1988

English Abstract
Integrated circuit dies (100) are **mounted** to the interconnection **leads** (160) on frames of tape automatic bonding (TAB) film (140). Thereafter, each frame of the TAB **film** (140) with the **attached integrated circuit** die (100) is affixed to an electrically insulating, thermally conductive plate (180, 900) to form a sandwich structure. A number of sandwich structures (300, 702...

...700) are selectively electrically connected to the interconnection leads (160) of other sandwiches in the stack (400, 700) to form a system of electrically interconnected **integrated circuits**. The system is compact and has short interconnection paths between **integrated circuits** (100) so that the propagation delays of signals between **integrated circuits** (100) are minimized.

Claim
1 1 An apparatus for interconnecting a plurality of **integrated circuits** (100) characterized by a stack (400,600,700) having a top surface, a bottom surface and a sidewall (706), said stack (400,600,700) comprising...

...stacked sandwiched structures (300,702), each sandwiched structure (300,,702) of at least a portion of said plurality of sandwiched structures (300,,702) comprising:
an **integrated circuit** die (100,1001,10011) having a plurality of **bonding pads** (120,1201,12011) on a surface thereof, said surface having an outer periphery ;
a first plurality of electrical conductors (160F160I)f said first plurality of electrical conductors (160,1601) electrically and mechanically **bonded** to said **bonding pads** (120,,120,1,,120") of said **integrated circuit** die (10OF1001,10011);
a first electrically insulating plate (180,900) adhesively bonded to said **integrated circuit** die (1000,100"O'100,I)f said first electrical insulating plate (180,900)- having an outer periphery with dimensions selected so that said outer periphery of said first electrically insulating plate (180,900) extends beyond the outer periphery of said surface of said **integrated circuit** die (100,1001,10011) and so that an exposed portion of each of said first plurality of electrical conductors (160,1601) extends

44/TI,PN,PD,PY,K/16 (Item 16 from file: 349)

PACKAGING SYSTEM FOR STACKING **INTEGRATED CIRCUITS**
SYSTEME DE CONDITIONNEMENT PERMETTANT D'EMPILER DES CIRCUIT INTEGRES
Patent and Priority Information (Country, Number, Date):
Patent: WO 8808203 A1 19881020
Publication Year: 1988

English Abstract
Integrated circuit dies (100) are **mounted** to the interconnection **leads** (160) on frames of tape automatic bonding (TAB) film (140). Thereafter, each frame of the TAB **film** (140) with the **attached integrated circuit** die (100) is affixed to an electrically insulating, thermally conductive plate (180, 900) to form a sandwich structure. A number of sandwich structures (300, 702...

...700) are selectively electrically connected to the interconnection leads (160) of other sandwiches in the stack (400, 700) to form a system of electrically interconnected **integrated circuits**. The system is compact and has short interconnection paths between **integrated circuits** (100) so that the propagation delays of signals between **integrated circuits** (100) are minimized.

Claim
1 1 An apparatus for interconnecting a plurality of **integrated circuits** (100) characterized by a stack (400,600,700) having a top surface, a bottom surface and a sidewall (706), said stack (400,600,700) comprising...

...stacked sandwiched structures (300,702), each sandwiched structure (300,,702) of at least a portion of said plurality of sandwiched structures (300,,702) comprising:
an **integrated circuit** die (100,1001,10011) having a plurality of **bonding pads** (120,1201,12011) on a surface thereof, said surface having an outer periphery ;
a first plurality of electrical conductors (16OF160I)f said first plurality of electrical conductors (160,1601) electrically and mechanically **bonded** to said **bonding pads** (120,,120,1,,120") of said **integrated circuit** die (10OF1001,10011);
a first electrically insulating plate (180,900) adhesively bonded to said **integrated circuit** die (1000,100"O'100,I)f said first electrical insulating plate (180,900)- having an outer periphery with dimensions selected so that said outer periphery of said first electrically insulating plate (180,900) extends beyond the outer periphery of said surface of said **integrated circuit** die (100,1001,10011) and so that an exposed portion of each of said first plurality of electrical conductors (160,1601) extends

44/TI,PN,PD,PY,K/17 (Item 17 from file: 349)

DOUBLE CAVITY SEMICONDUCTOR CHIP CARRIER
SUPPORT DE PLAQUETTE DE SEMI-CONDUCTEUR A DOUBLE CAVITES
Patent and Priority Information (Country, Number, Date):
Patent: WO 8100949 A1 19810402
Publication Year: 1981

Fulltext Availability:
Claims

English Abstract
...having a pair of semiconductor chip receiving cavities in the opposite faces thereof. The package enables mounting and electrical interconnection of a pair of semiconductor **integrated circuit** chips in a package of the same size as that for a single chip and having somewhat greater thickness. External terminals (93) on an outside face of the carrier are connected selectively by metallization paths (44, 53, 55, 83) integral with the carrier to **chip mounting** pads (41, 51) and to internal terminals (28) within the carrier. The internal terminals are disposed peripherally with respect to the chip cavities and adapted for interconnection with chip contact pads (26). Thus, a pair of unlike semiconductor **integrated circuits** can be interconnected in accordance with different patterns within a single package.